I-Connect007

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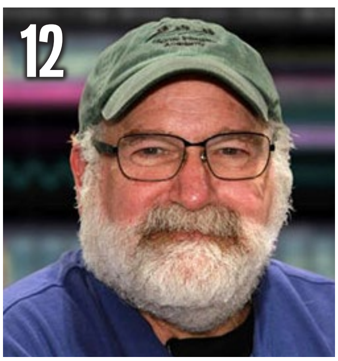
DESIGN007 MAGAZINE

DESIGN EDUCATION: Planning Your Next Move

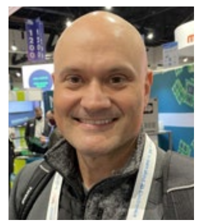
DESIGN007 MAGAZINE

Planning Your Design Education Strategy

There are more avenues for acquiring design education and training than ever before—live classes, online webinars, YouTube videos, and blogs, not to mention a variety of textbooks written by industry luminaires. But where should you start? We asked this month's contributors to share their advice for setting up a PCB design education and training plan that can take young PCB designers and design engineers through their entire careers.



FEATURE INTERVIEWS



FEATURE COLUMN

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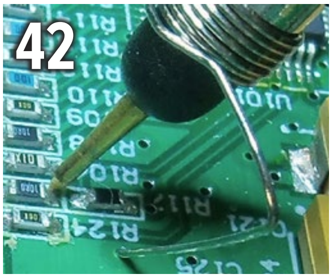

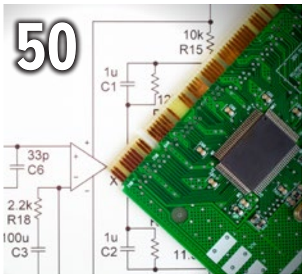

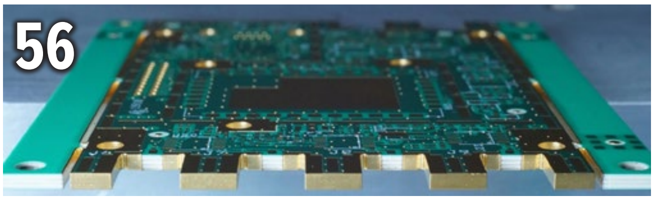

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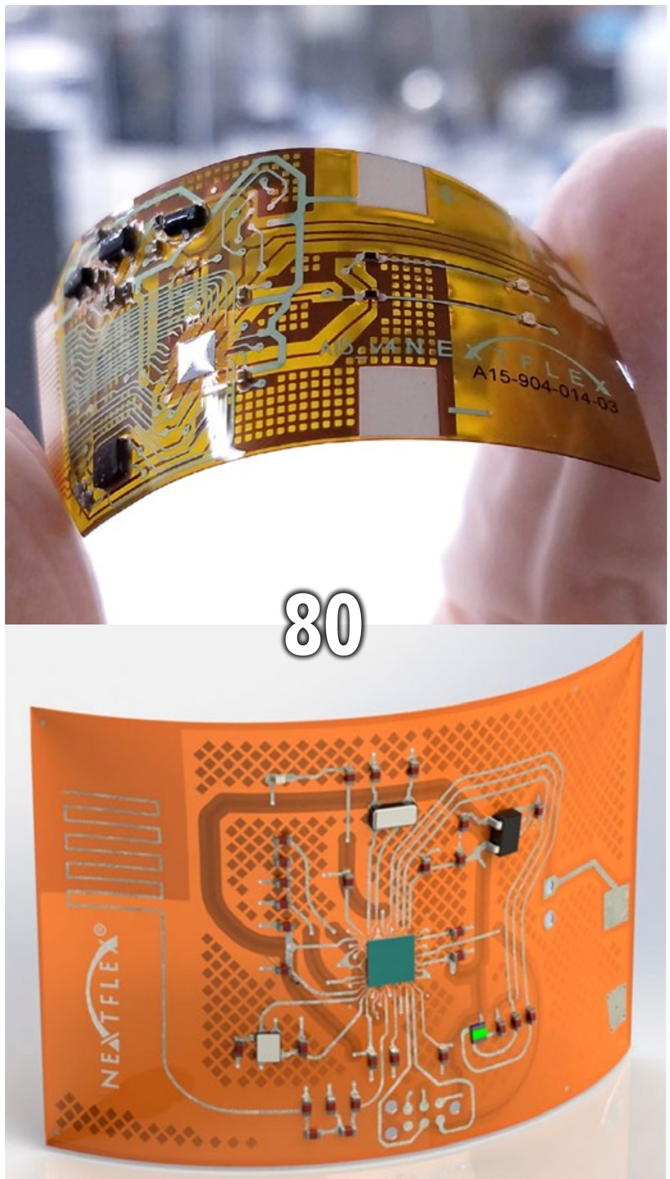
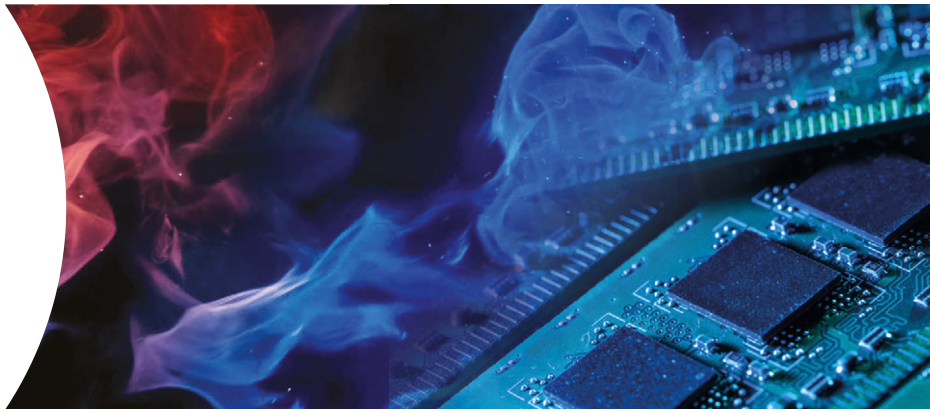
FLEX007

This Month in Flex

Flexible and rigid-flex circuits have become one of the mainstays of our everyday electronic devices. Now, flexible circuitry is serving as a stepping stone to further innovations, such as flexible electronics and flexible hybrid electronics. This month, we bring you articles by Joe Fjelstad and Sean Nachnani that cover the opportunities and challenges that these technologies present.





Plan Your Continuing PCB Design Education

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Congratulations! You've gotten your first job as a PCB designer or a design engineer. You're settling in, and learning your company's culture, as well as the culture of the global design community.

Welcome! We're glad to have you aboard, and we're not kidding. We've been waiting for you. In fact, we have enough similar openings across the industry to employ your entire graduating class and then some.

Now, we have some news: You may have graduated, but your education has only begun. Yes, it's time to set up a strategic plan for continuing your design education. This isn't an option—it's a necessity.

In a way, at least for the purposes of this column, designers are a lot like great white sharks. The *carcharodon carcharias* of "Jaws" fame will drown if he's not constantly swimming; likewise, designers will feel like they're drowning if they're not constantly working on their design education. You'll have to keep learning just to stay current, because the technology is constantly evolving.

You're very lucky: There are more avenues for acquiring design education and training than ever before. Not long ago, your only option—outside of buying books by Lee Ritchey, Eric Bogatin, Henry Ott, or Doug Brooks—was to attend an in-person design conference that might be 2,000 miles away. If your company didn't support your educational plans, you either missed out or you took vacation days and paid your own way.

But now designers have access to thousands of online classes (many of them free), as well as live, in-person courses at IPC APEX EXPO, DesignCon, the PCB Design Conferences, and regional tabletop shows such as PCB Carolina.

But even a cursory journey through the internet reveals that some of the online PCB design courses are just plain bad, particularly on YouTube. It's up to the dedicated design student to separate the wheat from the chaff, as your pastor might say. And how can you know what constitutes solid PCB design curriculum if you're a brand-new designer? It's all a bit overwhelming for a newcomer.

You don't want to waste time and effort bouncing around aimlessly from one design class to another. You need to plan your continuing PCB design education. Ideally, this plan will provide a framework for your future—a step-by-step strategy for your design education and training curriculum.

But where should you start?

We asked this month's contributors to share their advice for setting up a PCB design education and training plan that can take young PCB designers and design engineers through their entire careers. Many of this month's contributors have experience teaching at the college level as well as at industry conferences and trade shows.

In our first feature, signal integrity instructor Eric Bogatin explains how he helps his engineering students at University of Colorado-Boulder plan their college education. We also have an interview with Bill Brooks, a design instructor and former Palomar College adjunct professor, who details some of the educational milestones designers should set their sights on.

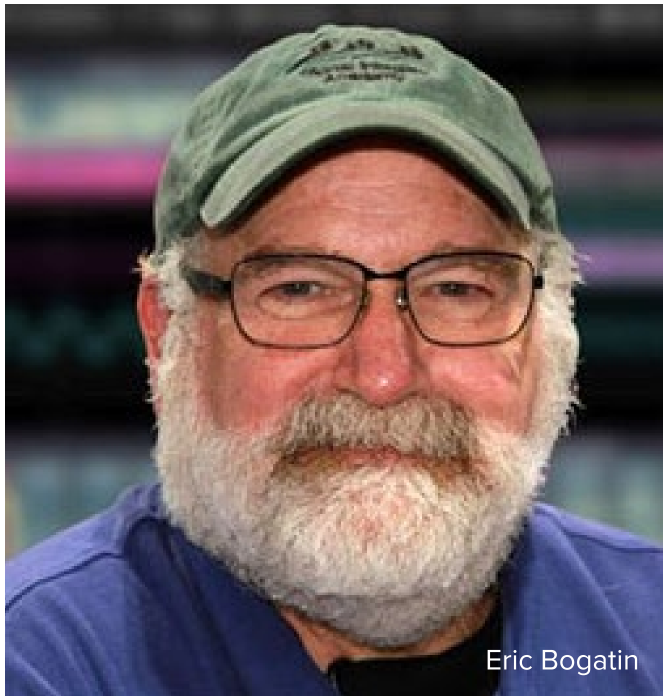
Next, we have a conversation with Rea Callender, Altium's new VP of education, who explains how to find the right classes and training for your skill set, and the role EDA vendors can play in training. And EDA engineer Ben Jordan lays out an educational outline for new designers, and he stresses why it's so important to take charge of your design education, whether your company supports you or not.

We also have articles by Anaya Vardya, Sean Nachnani, and Steve Hageman, as well as columns from our regular contributors Barry Olney, Tim Haag, Dan Feinberg, Phil Kinner, Matt Stephenson, Dave Wiens, and Joe Fjelstad.

See you next month! DESIGN007

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 20 years. He can be reached by clicking here.

Planning Your Design Education Strategy


Eric Bogatin

Feature Interview by Andy Shaughnessy
I-CONNECT007

There are (finally) some young people joining the PCB design and design engineering community. We're glad to see their youthful faces at trade shows and conferences. But if you're a recent grad and working in your first "real" job, you might be asking yourself: How do I set up an education and training plan for my career in PCB design? What's my next step?

We asked Eric Bogatin to weigh in with his thoughts. Eric has a unique viewpoint: He's a veteran signal integrity instructor, as well as a professor in the College of Engineering and Applied Science at the University of Colorado, Boulder. In this interview, Eric lays out some of his planning strategies and the need for a degree in electrical engineering in the PCB design world.

Andy Shaughnessy: Eric, how do you help your students plan their educational objectives at the college?

Eric Bogatin: This is an important question. It is never too early to start thinking about what your career goals are, either working in the industry or just as a student. If a student is not 100% clear and dedicated to a particular path, I encourage them to use the opportunity as an undergraduate to experiment and explore topics. They need to get enough experience to figure out what they like—design, measurement, software, simulation, circuits, fields, designing systems, working with people, working behind a computer, teaching, or something else.

Once they have a sense of what they really enjoy and a plan, then we select courses to help support that path. Because of the core courses most EE students need to take, there is not a lot of flexibility, but there are usually four or five electives that a student can select.

Shaughnessy: What criteria should designers keep in mind when evaluating their educational needs in the industry?

Bogatin: You need a balance between the fundamental principles and the hands-on experience applying these principles. Taking online classes is fine, but plan to get some kits so you can actually build and measure circuits. Taking some courses in which you will get experience designing and building reference designs will help build your confidence.

Shaughnessy: What would you advise to PCB designers who want to set up their own strategic learning plans?

Bogatin: If you want to be a PCB designer, rather than a circuit designer and hardware designer, then you probably don't need a BSEE degree. Just getting some electronics experience and training in designing and building some boards is good enough to get started. But if you are going to be a hardware engineer and take responsibility for the circuit design and do the board design, then a BSEE and lots of hands-on experience designing and building circuits is important. You cannot get too much experience building working circuits in a solderless breadboard to gain experience in debugging and characterizing circuits.

Shaughnessy: When I first started covering PCB design in the late '90s, there were no "critical paths" to becoming a designer. It sounds like a BSEE degree might not be that critical path unless someone is focusing on circuit design or hardware design.

Bogatin: That's right. If you are going to be a layout designer, I don't think you need a degree. However, the more classes you've taken, the more fundamental principles you understand, the higher your value as a layout designer. Experience working under a master is more important than a degree. However, if you are going to be a hardware engineer, then a BSEE degree is a must. Otherwise, you may not have the math skills needed to do circuit analysis.

Shaughnessy: Is there anything else you'd like to add?

Bogatin: Yes. Follow the path of Ikigai[1]. I think this is the secret to finding a fulfilling career path.

Shaughnessy: Thanks for your time, Eric.

Bogatin: Thank you, Andy. DESIGN007

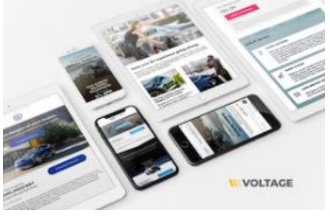
References

1. "The Philosophy of Ikigai: 3 Examples About Finding Purpose," by Jeffrey Gaines, PositivePsychology.com, Feb. 7, 2022.

Affinitiv Launches Electric Vehicle Division, Voltage

NEC has launched an Automation Ecosystem to bolster its 5G xHaul Transformation Services, bringing communication service providers (CSPs) simplified operations, cost effectiveness and faster time-to-value for their multi-vendor-based networks. The 5G xHaul Transformation Solutions and Services are part of NEC Open Networks, a suite of solutions for realizing the real-world benefits of truly open 5G networks.

Automation technologies will play a pivotal role in enabling efficient and reliable operations over increasingly complex transport networks. However, incorporating automation for a multi-vendor network environment will require new capabilities, such as holistically redesigning the network architecture and its processes by breaking the silos of traditional network domains and operationalizing them with software engineering skillsets.



Combining the network and software engineering capabilities built at the NEC 5G Transport Network Center of Excellence (CoE) with the expertise of these strategic partners, the ecosystem is aimed at providing robust automation solutions for the full lifecycle of 5G xHaul operations.

"Deploying Accedian's cloud-native agents assures the delivery of services and applications across distributed networks with real-time visibility to achieve operational consistency, integrated lifecycle management, and automated assurance for user experience-based closed-loop automation," said Richard Piasentin, Chief Strategy and Marketing Officer, Accedian.

(Source: ACN Network)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The Coupling Coup

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Coupling on a multilayer PCB may be a good or bad thing. On one hand, close coupling of signal traces to reference planes and differential pair signals is the best way to prevent common mode radiation and to mitigate electromagnetic (EM) emission. But on the other hand, close coupling of unrelated signal traces can bring us grief with unintentional crosstalk caused by overlapping EM fields. In this month's column, I will look at where close coupling should be used and where it should be avoided.

There are five common situations where coupling can influence the signal and power integrity of a design:

1. Signal to reference plane coupling.
2. Return path loop area.
3. Planar coupling,
4. Differential pair signal coupling.
5. Induced crosstalk.

1. Signal-to-reference Plane Coupling

The first rule of stackup design is that all signal layers should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path. Closely coupling a signal trace to the reference plane minimizes the loop area and reduces inductance. Also, reducing the dielectric height will result in a large reduction in crosstalk without having a negative impact on available space on your board. However, one must be aware that reducing the dielectric height will require an increase in trace width to accommodate the desired impedance of the transmission line. This could become an issue for a densely routed design. So, typically a ~3 mil thick dielectric is selected for microstrip configurations. Figure 1 illustrates the variation of dielectric thickness and trace width. For stripline configurations, the dielectric thickness generally falls

Layer No.	Via Span & Hole Diameter				Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
					Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5						
1	8	8	4	4	Signal	Top	Conductive			2.2	12	4	0.43	51.67	98.65
					Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9						
2					Plane	GND	Conductive			1.4					

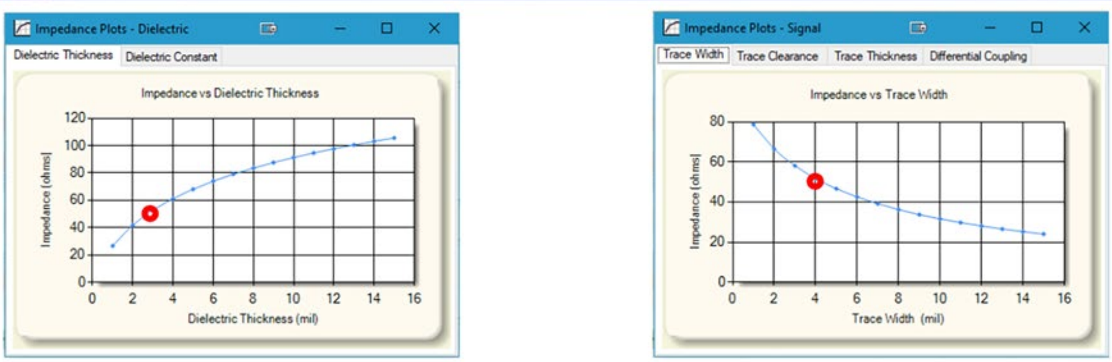
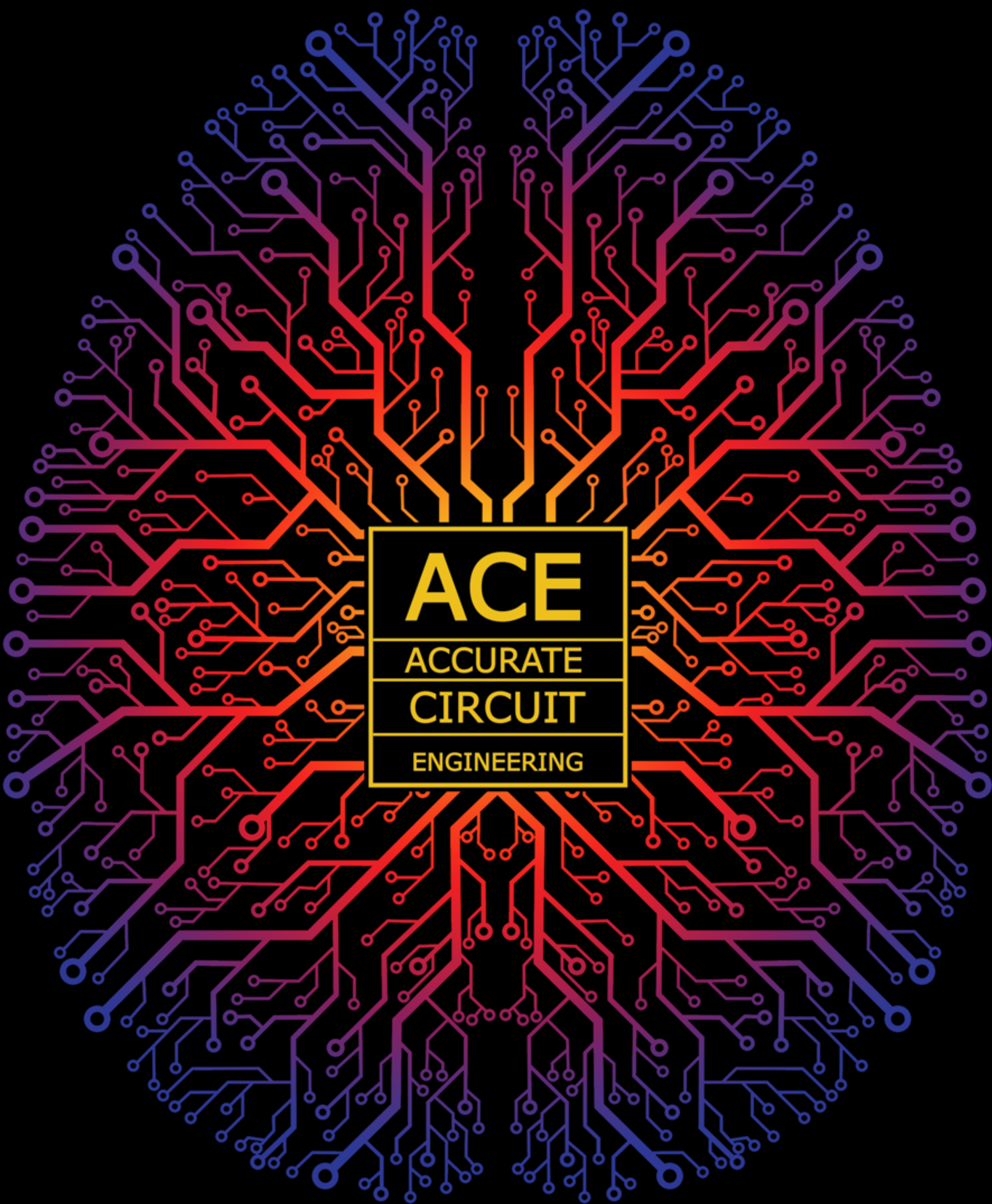


Figure 1: Coupling of signal-to-reference plane (simulated by the iCD Stackup Planner).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between 4–5 mils due to the proximity of the two planes.

2. Return Path Loop Area

Return path discontinuities (RPDs) can create large loop areas that increase series inductance, degrade signal integrity, and increase crosstalk and electromagnetic radiation. Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems. RPDs produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel to channel noise, and may promote mode conversion.

Common mode radiation is the result of parasitics in the circuit that emanate from the unwanted voltage drops in the conductors. As the signal follows the transmission line, capacitive coupling between the trace and plane conductors completes the loop and displacement current flows through the capacitance which returns to the source. The common mode current that flows through the ground impedance produces a voltage drop in the digital logic ground system and generates magnetic radiation.

To control common mode radiation, it is important to minimize the common mode ground voltage at the source. Also, good grounding minimizes noise sources by presenting common mode currents with a low impedance path to ground potential. Returning signal currents tend to stay near their signal conductors, falling off in intensity with the square of increasing distance. If the return path of a common mode current is far from the signal path, then the common mode current will radiate. However, if you engineer the return path to be near the source current, then the loop area will be small and therefore the common mode current will not radiate.

3. Planar Coupling

With the continuous trend to smaller feature sizes and faster signal speeds, planar capacitor laminate or embedded capacitor materials (ECM) are becoming a cost-effective solution for improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference. Coupling the planes very close together creates high capacitance.

Embedded capacitance technology allows for a very thin dielectric layer (0.24–2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1 GHz. Unfortunately, standard decoupling capacitors have little effect over 1 GHz and the only way to reduce the AC impedance of the power dis-

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded capacitance material	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High T_g epoxy based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi T_g	1.0
Integral Technology	Zeta Cap	Hi performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Sanmina	ZBC1000	Buried cap, hi performance decoupling	1.0
Sanmina	ZBC2000	Buried cap, hi performance decoupling	2.0

Table 1: Embedded capacitor materials available in the iCD Dielectric Materials Library.

tribution network above this frequency is to use ECM or, alternatively, die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and loss up to 15 GHz.

Planar capacitance requires a very thin dielectric with a high dielectric constant (Dk). This is contrary to the typical high-speed design that requires a low dielectric constant to improve dissipation losses. However, in this case, we need high capacitance, hence the high Dk. With 20 nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded-capacitance material on the market (Table 1).

4. Differential Pair Signal Coupling

Electromagnetic radiation from digital circuits can occur as either differential mode or common mode. Differential mode is typically equal and opposite, and therefore any radiating fields will cancel. Conversely, common mode radiation from two coupled conductors is identical. It does not cancel but rather reinforces. Unfortunately, differential mode propagation can be converted to common mode by parasitic capacitance, or any imbalance caused by signal skew, rise/fall time mismatch, or asymmetry in the channel. Also, return path discontinuities can create large common-mode loop areas that increase series inductance and electromagnetic radiation.

In the case of differential pairs, the transformation from differential mode to common mode typically takes place on bends and non-symmetrical routing, near via and pin obstructions, but can also be caused by small changes in impedance due to RPDs.

If a differential pair is well balanced, then tight coupling will achieve an effective degree of field cancellation. However, if they are not perfectly balanced (Figure 2), then the degree of cancellation is not determined by the spacing, but rather by the common-mode balance of the differential pair. Most digital drivers have poor common-mode balance and therefore differential pairs often radiate far more power in the common mode than in the differential mode. In such a case, one gains no radiation benefit from coupling the differential traces more closely together.

Differential signals that are closely coupled will operate mainly in the differential mode with some common-mode radiation from imbalances in the signals. If the two traces are separated enough to prevent coupling, then both act as single-ended signals. So, a 100-ohm differential pair becomes two individual 50 ohm single-ended signals. This is fine, providing the loop area is small and the impedance does not change along the length of the signals.

5. Induced Crosstalk

As signal traces come into proximity of an aggressor signal, part of that signal is unintentionally electromagnetically coupled into the victim trace as noise due to the overlapping of EM fields. Crosstalk is three-dimensional and is dependent on the signal trace separation, the

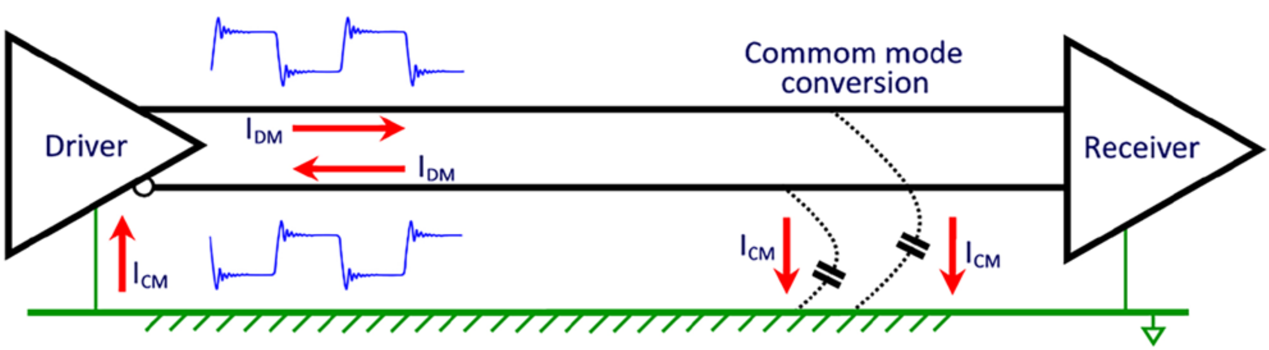


Figure 2: Differential mode signals can be converted to common mode.

trace to plane(s) separation, parallel segment length, the transmission line load, and the technology employed. But crosstalk also varies depending on the physical stackup configuration.

Crosstalk is caused by the coupling of electromagnetic fields. Electric fields cause signal voltages to capacitively couple into nearby traces. Capacitive coupling draws a surge of drive current which causes reflections on the transmission lines. Whereas magnetic fields cause signal currents to be induced into nearby traces, inductive coupling produces ground bounce and power supply noise. Crosstalk falls off rapidly with the square of the distance. The degree of impact is related to the aggressor signal voltage, available board real estate, and thus the proximity of signal traces.

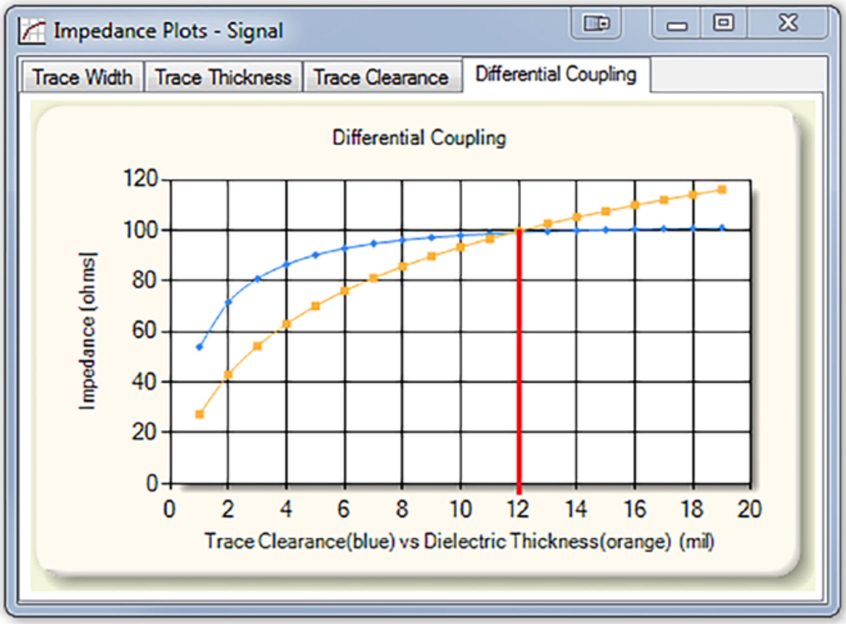


Figure 3: Coupling levels off above 12 mils separation (simulated by the iCD Stackup Planner).

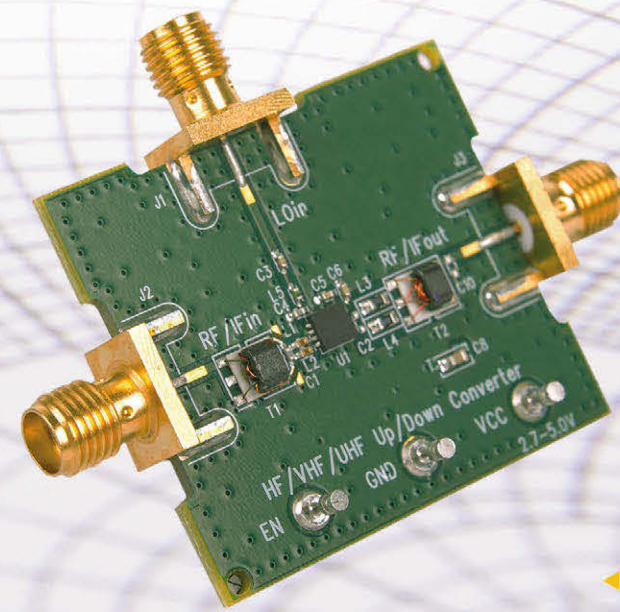
The easiest way to reduce crosstalk from a nearby aggressor signal is, of course, to increase the spacing between the signals in question. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level. However, crosstalk is determined by the ratio of the trace separation and the height of the trace above the plane. By varying the trace height, one can also control the coupling—hence crosstalk. If real estate is limited, then this may be a better solution rather than increasing routing density. A tight coupling (less height) results in less crosstalk.

There is a sweet spot where the total energy stored in the electromagnetic field surrounding the trace is optimized. Crosstalk between two or more conductors depends on their mutual inductance and mutual capacitance. The inductance plays a major role in this coupling. The signal return currents will generate EM fields. Those EM fields, in turn, induce voltages (crosstalk) into other signals.

It can be seen in Figure 3 that the differential impedance or the coupling of two parallel traces levels off at 100Ω above 12 mils trace clearance (blue curve). This is simulated quickly by multiple passes of the field solver. All other factors being equal, the differential impedance will always be 100Ω regardless of increased spacing. This also represents the point at which crosstalk (coupling) begins. This curve provides a clear map of the design space and efficiently defines the stackup configuration for single-ended and coupled pairs. In this case, once the separation is less than 12 mils, the two traces begin to couple and transfer electromagnetic energy.

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer but may also be broadside-coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area.

In conclusion, parasitic effects can be minimized by separating traces as much as possible, coupling signal traces close to the reference planes, reducing the loop area of return cur-


LOin
RF/IFout
RF/IFin
HF/VHF/UHF Up/Down Converter
VCC
2.7-5.0V
GND
EN

rent, using good stackup design practices, and by lowing the AC impedance of the PDN by using distributed embedded capacitance.

Key Points:

- The first rule of stackup design is that all signal layers should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path.
- Return path discontinuities (RPDs) can create large loop areas that increase series inductance, degrade signal integrity, and increase crosstalk and electromagnetic radiation.
- Common mode radiation is the result of parasitics in the circuit that emanate from the unwanted voltage drops in the conductors.
- If the return path of a common mode current is far from the signal path, then the common mode current will radiate.
- ECM technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference. Coupling the planes very close together creates high capacitance.
- ECM provide distributive decoupling capacitance that take the place of conventional discrete decoupling capacitors over 1 GHz.
- Differential mode propagation can be converted to common mode by parasitic capacitance or any imbalance caused by signal skew, rise/fall time mismatch, or asymmetry in the channel.
- In the case of differential pairs, the transformation from differential mode to common mode typically takes place on bends and non-symmetrical routing, near via and pin obstructions, but can also be caused by small changes in impedance due to RPDs.
- Differential signals that are closely coupled will operate mainly in the differential mode with some common-mode radiation from imbalances in the signals.
- If the two traces of a differential pair are separated enough, to prevent coupling, then both act as single-ended signals.
- As signal traces come into proximity of an aggressor signal, part of that signal is unintentionally electromagnetically coupled into the victim trace as noise, due to the overlapping of EM fields.
- The easiest way to reduce crosstalk from a nearby aggressor signal is, of course, to increase the spacing between the signals in question.
- By varying the trace height, one can also control the coupling—hence crosstalk. If real estate is limited, then this may be a better solution.
- Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer but may also be broadside-coupled from the adjacent layer. DESIGN007

Columns by Barry Olney

- "Stackup Configurations to Mitigate Crosstalk"
- "The Dark Side—Return of the Signal"
- "Stackup Planning, Part 1"
- "The Curse of the Golden Board"
- "Material Selection for SERDES Design"
- "Common Symptoms of Common Mode Radiation"

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, click here.

Take Charge of Your PCB Design Education

Feature Interview by Andy Shaughnessy
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Ben Jordan is an electrical engineer who's passionate about PCB design. He also teaches a variety of classes on topics such as PCB design, RF and microwave design, and antenna theory. For this issue, we asked Ben to share his advice for PCB designers who are interested in planning their lifelong design education strategy.

Andy Shaughnessy: You've been a PCB design instructor for years now. What advice would you give young PCB designers who would like to set up their own strategic learning plans and educational objectives?

Ben Jordan: Know that it's going to take time. Be willing to invest in yourself with a multi-step plan that starts with your basic electronics and builds on that toward industry certification. You'll need to acquire at least a moderate hobby level of electronics knowledge, get to know the tools, manufacturing processes, and ultimately walk through it all with real-world experience. That experience can be done on your own and with your own projects, but for some learners it's probably wise to seek an internship where you'll have a mentor to guide you. I know some top-notch online courses where you will build the thing being discussed, so you can finish with a high level of confidence. You know your stuff and can present it as real work in your resumé or portfolio. You get the added benefit of knowing the effort and time that went into it, so you can begin to predict time and difficulty for future design projects.

Shaughnessy: What are some of the milestones in PCB design education and training that someone should shoot for?

Jordan: Ideally, get at least an associate's degree in electrical engineering from a local community college, if not a full bachelor's degree. A second-best would be a science degree with electives that teach you the physics of electronics and material science. I suggest this because, though not strictly necessary, it is an automatic shortcut to understanding sche-

matics, electronic components, and the fundamentals of propagation. Unfortunately, colleges still don't generally teach PCB layout and how signals work in circuit boards; Eric Bogatin's classes at the University of Colorado, Boulder are the exception. If you don't want to study at college, just find a good course on electronics for beginners. André LaMothe has a fantastic class on Udemy. It's so affordable that anyone can take it using free or open-source software along the way. It's really never been easier.

As a milestone, I recommend walking through specific ECAD tutorials. There are so many available, both free and paid. Learn a tool, preferably a commercial tool, if it's a career you want. Open-source tools like KiCAD have come an incredibly long way and are getting better, but honestly, the companies willing to pay you good money for design want it done in commercial tools. Use the job search function on LinkedIn to determine which tool is most in demand, then get an evaluation. Commit yourself for three to four weeks (whatever the evaluation period is), spending eight hours a day learning the software, watching videos, stepping through tutorials, and documentation. It's a big commitment but you will need to do it. The same goes for anyone who is looking to get a new job or contract with a company that has a different ECAD tool that you haven't used before.

The next milestone can be in tandem with the first one: Tour a PCB fabricator followed by an assembler. If there isn't one close to you, do the next best thing and watch some video tours on YouTube. Many of the best fabricators and assembly service providers have video playlists which will walk you step-by-step through the entire start-to-finish process. This step is critical. Too many engineers are designing hardware and the PCBs are far less than optimal or even have errors that require redesign, because the designer did not have a clear understanding of the manufacturing processes involved or the manufacturing limitations.

Ben Jordan

Finally, with a few actual working designs under your belt, get certified. This is the final goal because it confirms you know what you're doing, and you can be counted on to design boards that work right, and usually without revisions. There are two certifications available. For the longest time, the only one available was the IPC CID and CID+ (advanced). If you take that route, you will want to do CID first, with CID+ done a minimum of six months later. Basically, the CID+ was built by the most respected and experienced design gurus in the industry. I highly recommend it (I've taken it myself). Your newer second option for certification is with PCEA. Because the association is so new, not as many employers are aware of it or asking for this certification. However, it is a newer consolidated version of CID+ done by mostly the same people, now separated from IPC. Certifications cost $2,000 to $3,000, but it's worth it. The knowledge you gain in certification classes can't be learned anywhere but through the school of hard knocks.

I see it this way: You could do a Udemy electronics course for $12, spend another $2,000 to 3,000 to design and build projects (these are tax-deductible education costs), then another $2,000 to 3,000 on a certification. At most, you've spent $6,000 for an education that will pay you back in spades. You could go to a university and spend $30,000 to $100,000 depending on which one you go to, just for an honors EE degree where they still won't teach you PCB layout or the issues of manufacturing. Don't get me wrong: I value my bachelor's in engineering, but just think about the ROI on this.

Shaughnessy: What criteria should designers keep in mind when evaluating their educational needs, strengths, and weaknesses to stay on top of their game in the industry?

Jordan: What is it you see yourself doing long term? What is it you want out of life? If you find deep flow and satisfaction in designing and solving puzzles, double down on your PCB design education. If you want to chase big dollars and you have a "people" personality, get the technical knowledge and experience first, then focus on learning to sell or market PCB design or manufacturing services. That's a nice mix of commission while staying close to the technology. If you find you're most passionate about the actual electronic function of hardware, you might decide you really should do that degree and get deeper into the electromagnetic principles; you would need that, for instance, if you want to become a full-time microwave or RF engineer. All these decisions are different levels of financial and mental commitment. Doing engineering math is hard. Learning to sell is (arguably) just as hard, but you need to be open-minded and think where you want to go.

Shaughnessy: When I first started covering PCB design in the late '90s, there were no "critical paths" to becoming a designer. Is an engineering degree becoming the critical path for future designers?

Jordan: Strictly speaking, I don't think so. As I mentioned, if you are disciplined and passionate, you can learn what you need for designing PCBs from Udemy and the PCB industry certifications. But there will be gaps if you ever wanted to go deeper. Most people do not stay in the same career longer than three to four years these days, but for PCB and hardware electronics design, which seems to me to be a little bit different, because the kind of person who thinks of doing this in the first place usually is already becoming very passionate about it. Many PCB designers stay in this groove for decades, and never get bored. Every PCB design is like a brand-new job. But if you want to be a millionaire someday, you must face the fact you'll probably need to matriculate to being a business owner, salesperson, or something else down the road. If that's you, be sure you make room for that in your life plan.

Doing engineering math is hard. Learning to sell is (arguably) just as hard, but you need to be open-minded and think where you want to go.

Shaughnessy: Any final thoughts?

Jordan: Personally, I love PCB design, product engineering, embedded software development, and the whole nine yards. There are few careers that offer the interesting breadth of creativity that PCB and hardware design provide. But I'm currently crossing the chasm into being an entrepreneur. Please, wish me luck.

Shaughnessy: Best of luck, Ben! Thanks for your time.

Jordan: Thank you, Andy. DESIGN007

PCB007 Highlights

Nano Dimension's Board of Directors Welcomes Igal Rotem ▸

Nano Dimension Ltd., an industry leader in printing technologies, additively manufactured electronics, printed electronics, and micro additive manufacturing, announced the appointment of Mr. Igal Rotem to its Board of Directors.

It's Only Common Sense: The Show is Done, So Now What? ▸

If you attended IPC APEX EXPO, you probably made a lot of good contacts, talked to a lot of people, spent time with potential customers trying to convince them to buy your goods and services, or with vendors trying to figure out what equipment and services would be good for your company.

Cirexx Adds to Excellon Cobra Laser Fleet ▸

Cirexx International announced that they have acquired and installed a fifth Excellon Cobra laser machine. The hybrid Laser is equipped with both CO2 and UV laser technology.

Real Time with... IPC APEX EXPO 2022: The Supply Chain and Markets ▸

Pete Starkey interviews Mark Goodwin, COO of Ventec International, on the impact of the current supply chain condition. Their conversation also covers aerospace and the U.S. market.

Insulectro Appoints Industry Veterans Joan Vrtis and Jeff Doubrava to Advisory Board ▸

Insulectro, distributor of materials for use in the printed circuit board and printed electronics industries, has announced the appointment of Joan Vrtis and Jeff Doubrava to its advisory board.

Real Time with... IPC APEX EXPO: PCB Manufacturing Today ▸

Dick Crowe speaks with Kurt Palmer, president of Burkle North America, about the trends he sees in PCB manufacturing today. From LDI to laser drills, they discuss a wide range of concerns and opportunities.

Altix Receives Direct Imaging Order for Fine Line Prototyping ▸

Altix is delighted to announce that the CEA-Liten has ordered an Adix SA for fine line applications to be part of their research activities focused on micro and nano-technologies, smart digital systems and renewable energy.

IPC Honors Apple, MacDermid Alpha Electronic Solutions with Corporate Recognition Awards ▸

IPC presented its highest corporate honors to two IPC member companies, Apple Inc., and MacDermid Alpha Electronic Solutions during the IPC Annual Meeting/Awards Ceremony at IPC APEX EXPO 2022.

Gardien Group Unveils New Functionality and Software for Embedded Components Test ▸

Historically the testing of embedded resistors and/or capacitors has been a tedious ordeal. Gardien Group now offers an automated solution on their line of flying probe testers using their new FPX software platform.

Planning Your Design Education: Keep an Open Mind

Feature Interview by Andy Shaughnessy
I-CONNECT007

Rea Callender is the new vice president of education for Altium. He has a background in business development and entrepreneurship, along with experience in K-12 education. This seemed like a pretty good combination, so I asked Rea to share his thoughts on the best avenues for design education, as well as strategies for setting up a lifelong PCB design education plan.

Andy Shaughnessy: What advice do you have for PCB designers who would like to set up their own strategic learning plans for their career in design?

Rea Callender: Technology moves very quickly, and it can be difficult for designers to keep up with the technological developments that are most relevant to them specifically. The first place to start is obviously to keep up with developments from CAD vendors who are constantly updating versions of their software and tools. The new features they announce can help you be more efficient.

We also recommend that designers subscribe to some electronics industry publications. PCB publications are important, but there are other publications that can give you an inside view of new technologies as they start to hit the market. These publications can also give you access to webinars, white papers, eBooks, conference notifications, exclusive articles with useful design information, and more.

Shaughnessy: What criteria should designers keep in mind when evaluating their educational needs in the industry?

Callender: Probably most important is to keep an open mind and take advantage of resources—because you find them interesting, not just because you need them for your job. You never know what you'll learn in a webinar, conference, or free workshop. Because board designers participate in a lot more than board

Rea Callender

design, having well-rounded exposure to other areas of electronics really helps you excel in complex projects.

Shaughnessy: When I first started covering PCB design in the late '90s, there were no "critical paths" to becoming a designer. Is an engineering degree becoming the critical path for future designers?

Callender: In many ways, a bachelor's engineering degree still provides an important foundation and is part of that critical path for prospective electronics designers. Today's designers are doing a lot more than PCB layout, so they need to have additional engineering training, and skills that go beyond use of CAD tools. Designers are participating in front-end engineering, circuit design and simulation, firmware development, test engineering, and even mechanical design. An engineering degree still provides excellent preparation for these areas of electronics design. However, many traditional engineering degrees are lacking instructional content on physical layout, DFM, and especially manufacturing.

Our view is that an industry-sponsored educational program focusing on PCB design can complement traditional electronics engineering degree programs. If you think about the entire design process, it's easy to see the link between the traditional front-end electronics engineering tasks, back-end application development, and the intermediate physical layout tasks in electronics design; it's all part of the broader product development process, and that's where designers excel. We believe the critical path forward is a mix of three paths: traditional engineering courses, general PCB design courses, and some tool-specific courses.

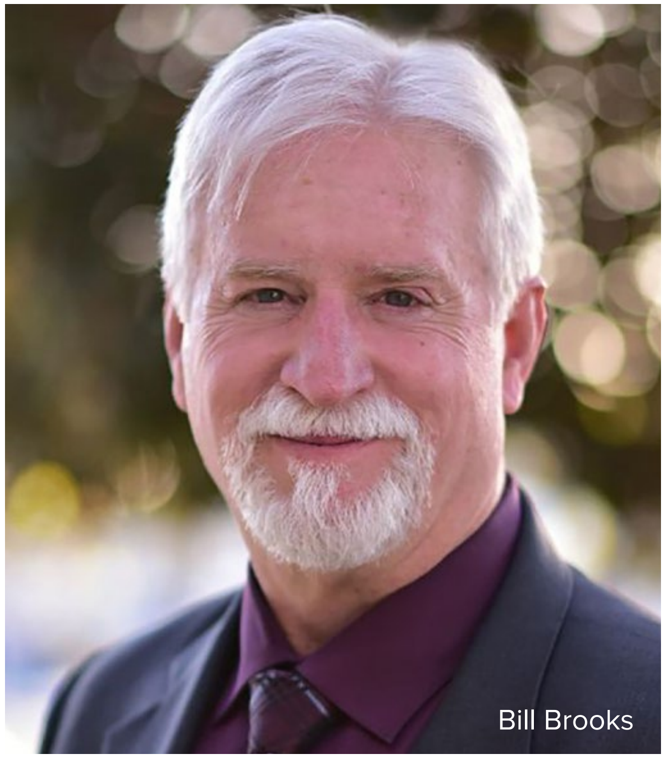
Shaughnessy: Is there anything else you'd like to add?

Callender: Pardon me while I share a few shameless plugs, some of them free of charge. Altium's Professional Training and Certification offers instructor-led and on-demand training options for anyone looking to expand their Altium Designer skills and knowledge. Altium Education provides free online curriculum and certification program for college and university students interested in electronics design, and it includes a free license of Altium Designer. And Upverter Education offers free online PCB design courses that take high school students through the electronic design process. Students have access to Upverter, a free web-based tool for designing electronics.

Shaughnessy: Sounds good. Thank you, Rea.

Callender: Thank you, Andy. DESIGN007

Setting Goals for Your PCB Design Education


Bill Brooks

Feature Interview by Andy Shaughnessy
I-CONNECT007

For this issue on planning your design education, we spoke with Bill Brooks of Nordson ASYMTEK, a long-time PCB designer, CID instructor, and fantastic sculptor. He is also one of the first to ever teach standalone PCB design courses in a college.

After he earned his certification to teach the IPC CID workshops, Bill served as an adjunct instructor at Palomar College near San Diego, teaching beginning and advanced PCB design classes for 10 years. I asked Bill to share his thoughts on setting up a PCB design education career plan, and the need to stay on top of your game as a PCB designer.

Andy Shaughnessy: You've had experience teaching PCB design at the college level, as well as decades of industry experience. When you were teaching, how did you help your students plan their educational objectives?

Bill Brooks: When I was teaching at Palomar College, each student wanted something different out of the education and curriculum. Some students were looking to enhance their existing experience by adding PCB design to their electronics knowledge base. Some were trying to gain the necessary skills to get a specific job designing PCBs in the electronics industry, and some were taking my classes to fill out a degree program at the college without ever using the knowledge in our industry.

We helped them define their personal objectives by asking questions about their personal goals. Then we offered the entire class the goal of achieving certification through the IPC Designers Council. Before you start a journey, it's a good idea to know where you want to go, develop a plan to get there, execute that plan, evaluate your progress, and make any adjustments along the way.

Shaughnessy: What would you advise to PCB designers who want to set up their own strategic learning plans and educational objectives?

Brooks: Understand where the industry is headed and prepare for the skills you will need to place yourself as an asset in the industry. Ask questions of the experts in the field, connect with others who are going the same direction. Never stop learning; be curious.

Shaughnessy: What criteria should designers keep in mind when evaluating their educational needs to stay on top of their game in the industry?

Brooks: Printed circuit design methods and knowledge are not static. Learn about the resources available from authors, industry experts, manufacturers, and assembly houses. Help educate yourself and then stay connected.

Shaughnessy: When I first started covering PCB design in the late '90s, there were no "critical paths" to becoming a designer. Is an engineering degree becoming the critical path for future designers?

Brooks: No. Though many aspects of PCB design are engineering tasks, an engineering degree is not required for much of what we do. There are good tools out there to help and having an interest in solving puzzles is more useful than knowing transistor theory.

Shaughnessy: Is there anything else you'd like to add?

Brooks: Get to work.

Shaughnessy: Good advice. Thanks, Bill.

Brooks: Thank you, Andy. DESIGN007

All Systems Go!

Ensuring Power Integrity: Explore, Design, and Verify

By Brad Griffin

When designing an electronic system, ensuring power integrity (PI) is all about making sure that the power you are putting into the system via the voltage regulator module (VRM) reaches the downstream components in an efficient, sufficient, and stable manner.

In the not-so-distant past, ensuring the PI of an electronic system was a relatively simple and pain-free task. Many products involved a single PCB populated by readily available off-the-shelf ICs, such as the classic 7400-series devices from Texas Instruments. For the purposes of PI, these ICs, which were presented in low pin count, coarse pin pitch packages could be treated as closed boxes represented by simple power models.

Meanwhile, in the case of traditional multi-board systems, the boards were typically plugged into—and powered by—a common backplane. This meant that, from a PI perspective, so long as each board met its total power budget, the boards could be largely designed and verified in isolation.


Brad Griffin

Time marches on and so things have indeed changed. Many of today's electronic designs feature multiple PCBs connected directly together, where each board may be populated by a mix of discrete components, off-the-shelf ICs and custom system-on-chip (SoC) devices. These high-capacity, high-performance, high pin count, fine pin pitch ICs and SoCs have sophisticated PI models associated with them. Many boards also feature system-in-package (SiP) devices in which multiple chiplets (unpackaged silicon die) are mounted on a common interposer and presented in a single package. Such interposers may be formed from a variety of materials, with silicon providing the finest features and highest interconnect densities. Each SiP may be considered as a small, specialized board in its own right. In the case of this class of design, at some stage PI will have to be performed on the entire system, including all the ICs, SoCs, SiPs, PCBs, connectors and cables.

To read this entire column, click here.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Gremlin Avoidance Tactics to Improve Productivity

Tim's Takeaways

by Tim Haag, FIRST PAGE SAGE

Sometimes I am envious of those who work with steel, on a construction site, or even tilling the earth. All these are tangible activities: you mold the steel, build a house, or harvest a crop. Instead, I work in electronics. Most of the time it is a good life, but every now and then a nasty little gremlin will pop up its ugly head and mock me. It could be a circuit that just won't give me the performance that I need, a short I can't find, or worst of all, an intermittent problem that just won't go away.

Case in point: I have a pickup truck nicknamed "The Beast" due to its size and capabilities. The Beast has served us well hauling dirt, rocks, and construction supplies, along with moving furniture and treasures for family members and friends alike as it pulls our trailer all over the Pacific Northwest. However, a few months ago The Beast's alarm system woke up the neighborhood at 2 a.m., even though there wasn't anyone near it. After a cursory examination, I quickly realized that any attempt to find and correct the problem with the alarm was way beyond my capabilities, and I left the truck in the care of my regular auto repair shop. Armed with an array of computerized diagnostic equipment, the repair shop went to work, starting off with several days of testing and debugging. After replacing the standard door switch, which didn't fix the problem, they worked through the host of other electronic components in the alarm chain. Finally, the decision was made to replace a thousand-dollar control module, and after some final diagnostics, the problem was resolved; or so everyone thought.

Now I know that this part of the story will sound made up,

but I swear its truth; I hadn't had the truck home but five minutes before that horrible alarm went off on its own again. I went back outside, checked it, and sure enough, the truck didn't chirp when I used the key fob to lock the doors. This is a sure indication that the control module thinks the door is still open even though it was closed. I went back inside to call my mechanic, and I kid you not, the truck's alarm went off again while I was on the phone with them. It felt like The Beast was deliberately mocking me.

I hadn't had the truck home but five minutes before that horrible alarm went off on its own again.

I know that everyone has dealt with their own gremlins in life. Those annoying little bugs and problems that creep up and cause us to spend a lot of time and money fixing a problem that just won't go away, and ultimately spoiling the weekend we had planned. What's worse, though, is when those glitches happen while on the job, causing us to go over budget and miss scheduled design and production deadlines. How many of us have waited for an answer from technical support when a CAD tool doesn't behave as expected, or you just can't find the intermittent short that you've spent all morning searching for? I know that I've been in those situations, and here's a couple ideas I've found that have helped me work through these annoyances.

Be Mentally Prepared

Gremlins usually appear at inopportune moments in our lives, and often create a lot of stress, anxiety, and even anger inside if we don't deal with it in a healthy way. If left unchecked, these emotions can derail our concentration and we'll lose the ability to focus on finding a solution to the problem. This is where the adage of "just walk away from it" can be a real lifesaver. If we resist the urge to yield to frustration when confronted with one of these problems and take a short break, it's amazing how our perspective can change. Sometimes the answer will be an obvious solution that we couldn't see because we were simply too close to the problem.

Let's face it, electronics will falter, CAD systems will develop glitches, and alarm systems will go off in the middle of the night. None of us know when the next gremlin will strike, so prepare yourself now for that eventuality to preserve your sanity. Allowing frustration to take the lead from our normal analytical approach to problem solving isn't a very practical or productive response to an unexpected gremlin. And for goodness sakes, be kind to yourself. After all, if you didn't break it in the first place, don't blame yourself if it's broken. Just step back a bit, take a deep breath, and then reevaluate the problem with a new perspective and a fresh pair of eyes. It's amazing how many times a resolution will present itself after just a short break.

Be Functionally Prepared

One of the things that can be so frustrating about gremlins is how they easily pop into our lives when we least expect them. As we just talked about, we can keep these unexpected annoyances from driving us nuts with some mental preparation. But is there anything that would help us on the more practical side? I think so. Consider the following:

- **Back up your work:** One of the most annoying gremlins is lost data. Sure, we've probably all deleted a CAD file that we didn't mean to or worked from the wrong database. But there are plenty of instances where a file becomes corrupt or is just plain gone when it shouldn't have been. To keep these gremlins at bay, make sure to regularly backup your work.

- **Establish a workflow:** Gremlins also seem to flourish in chaos and confusion. Whether by user error or a true computer glitch, work will get deleted, items will be forgotten, and data will be corrupted. You can help mitigate these gremlins by developing an established workflow which will ensure that each milestone is accomplished and checked off as you go. This will help reduce the confusion and give you tangible recovery points that you can go back to if necessary.

- **Communicate:** Make sure that you and your co-workers are on the same page. Many times, the problems in the workplace attributed to gremlins are more human in origin. Missing files and lost data may have simply been a case of the project being re-homed by another designer.

- **Ask questions:** Technical support is a wonderful thing, but there are many other channels of information available to you as well. FAQs, designer forums, white papers, and blogs are all available to you and can often provide quick answers to resolve some of these annoyances.

- **When in doubt, document it:** Keep track of your technical issues. Maybe you will find a common thread that will help diagnose a reoccurring gremlin, or at the very least, back you up in the event of a truly unknown gremlin. Trying to blame a missed deadline on a computer glitch without proof is sort of like saying the dog ate your homework. Document it.

Thankfully, improvements are being made all the time in the tools we are using and in design workflows. This month's edition of *Design007 Magazine* is full of examples of advances, opportunities, and new tool technologies to help PCB designers ascend to higher levels of excellence in their roles. With all the enhancements that are coming down the line, who knows but maybe we'll finally chase the gremlins out of the workplace for good.

I have one last piece of advice that might be helpful. Sometimes those pesky gremlins aren't supernatural apparitions at all, but instead are a simple mistake. Always take the time to check and double-check these glitches before you do anything rash. It can save you a lot of trouble, like starting over a design from scratch because you didn't realize that the database was simply in a different directory (my hand is up on this one).

Remember the gremlin that attacked my truck in the form of a faulty alarm system? As it turns out, when the shop first installed the new door switch, no one noticed they had been given the wrong part from their supplier. The door switch was the same size and shape as the original part, but it was slightly different internally, causing it to behave intermittently. But since the shop had ruled out a bad switch as the source of the problem by replacing it, they proceeded to search for other causes. It was only after I brought the truck back the second time and they started the diagnostic process all over from the beginning that they discovered they had the wrong door switch. The truck works great now, my money was refunded, and my mechanic has a new step in their workflow to double-check incoming part numbers. So don't be hasty when confronted with a gremlin and work through the problem thoroughly. Until next time, everyone, keep on designing. **DESIGN007**

Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns or contact Haag, click here.

Does Copper Pour on a Signal Layer Decrease Signal-to-signal Isolation?

Article by Steve Hageman
ANALOG HOME

Does putting a ground pour on PCB signal layers make the isolation better or worse? It can go either way, but with the proper knowledge and application, this technique will improve your designs.

In this article, I'll discuss how to simulate trace-to-trace isolation with true electromagnetic simulation software. We'll also cover a variety of rules of thumb that can help you stay away from trouble.

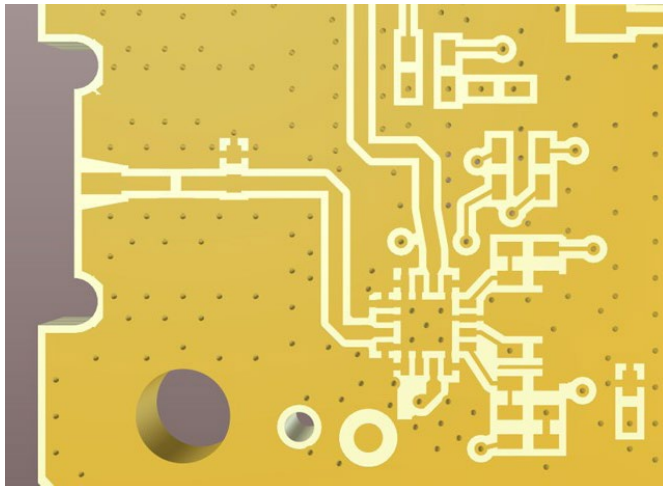


Figure 1: Many RF boards are built with CPWG construction because it offers much-improved EM performance. By improved, I mean smaller, less radiation, and better crosstalk performance than microstrip construction. This is essentially a copper pour on a signal layer and it works well, or legions of RF engineers would not be using it.

Fact or Fiction?

Recently an acquaintance told me, "I have heard that putting a copper pour on a signal layer between traces actually makes the isolation between the traces worse." I grabbed one of my RF boards (see Figure 1) and said, "If that is so, then how do all these RF boards that I have done with co-planar waveguide over ground manage to function? They all have copper pours on the signal layer, and they work to very high frequencies."[1]

Since co-planar waveguide over ground (CPWG), which is essentially "pouring copper on a signal layer," is used for a lot of RF work[2], and is proven to work for very high-performance RF circuits, how did this contradictory opinion catch on in the industry?

To investigate this, I used a one-inch section of 50-ohm microstrip consisting of an aggressor trace from ports 1 to 2 and a victim trace running in parallel from ports 3 to 4 as shown in Figure 2. I used typical values for the dimensions as might be on a real PCB. The trace width is 20 mils, with a spacing of 60 mils from

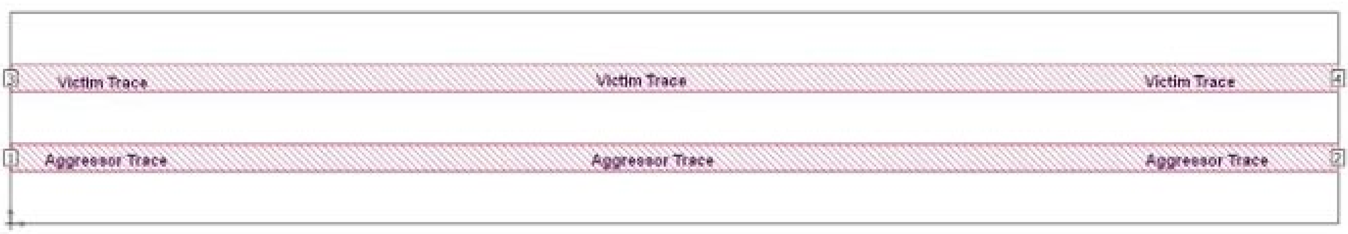
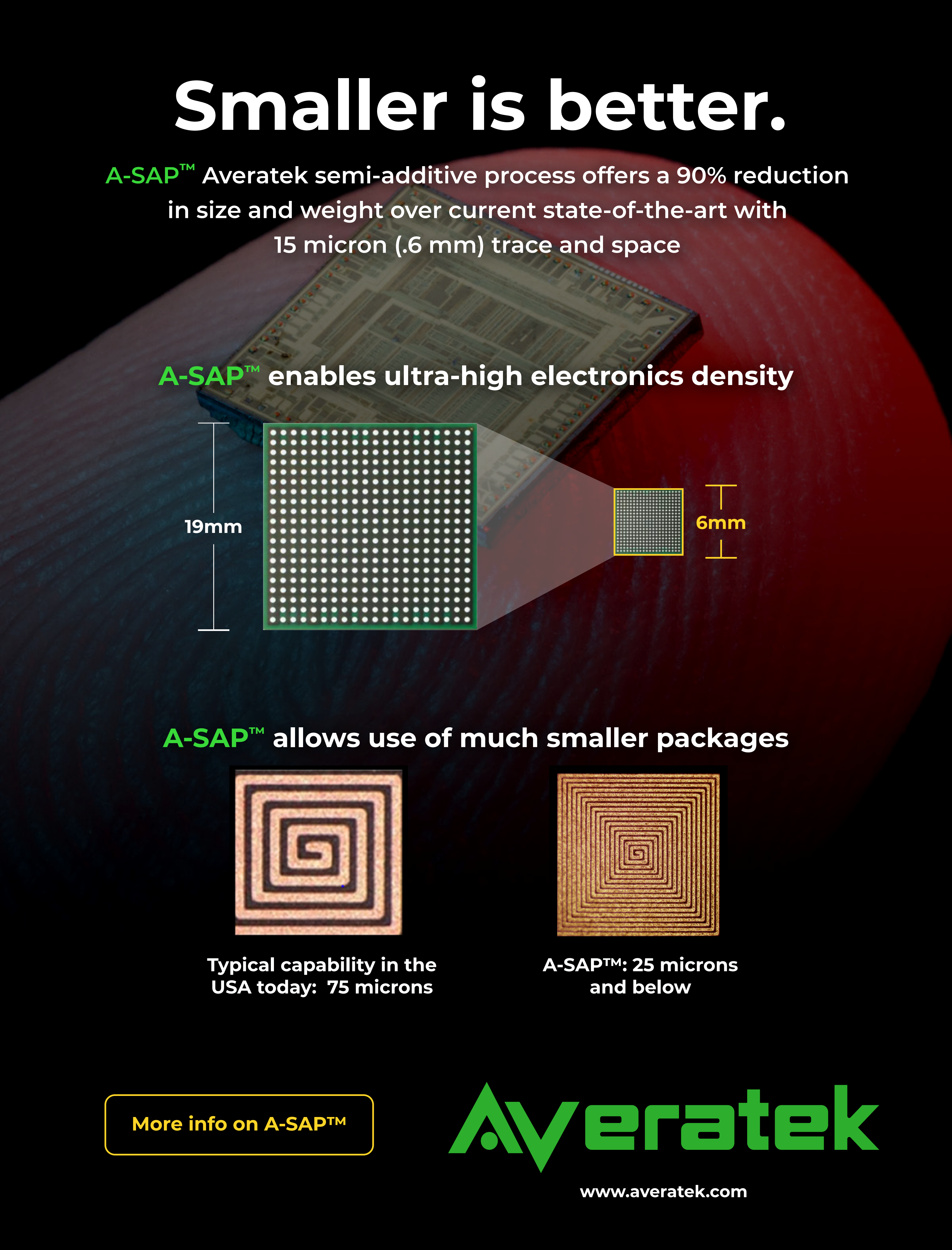


Figure 2: This 1-inch, 50-ohm aggressor trace (port 1 to 2) and victim trace (port 3 to 4) structure was modeled in Sonnet to study the effects of coupling between the traces.


Smaller is better.
A-SAP™ Averatek semi-additive process offers a 90% reduction in size and weight over current state-of-the-art with 15 micron (.6 mm) trace and space
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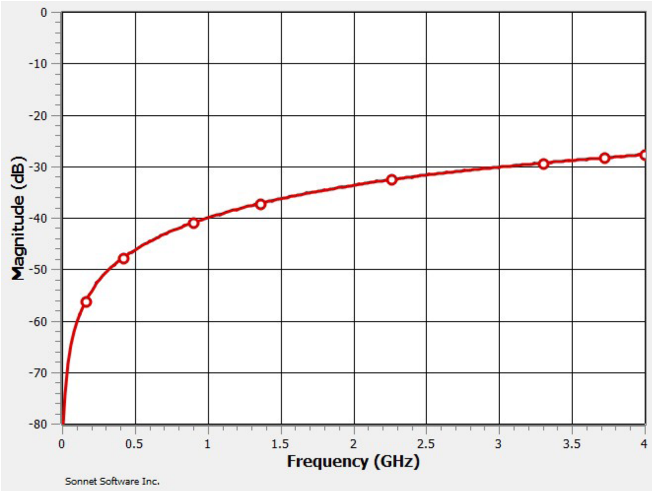


Figure 3: Simulating port 1 to port 4 coupling of the structure shown in Figure 2 shows nothing strange in the frequency range of 0-4 GHz.

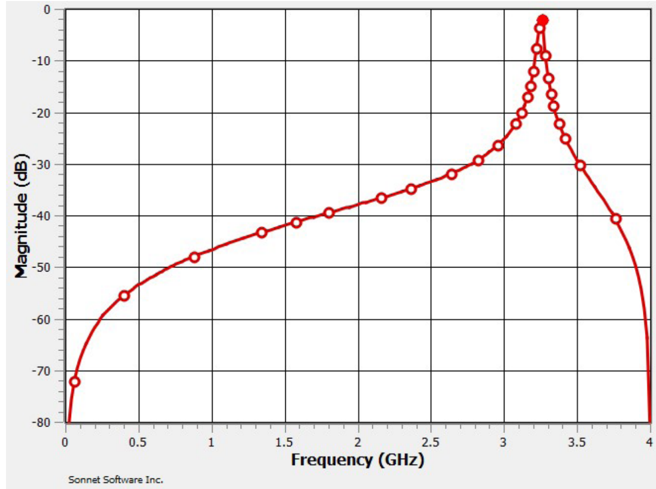


Figure 5: The resulting coupling measurement from ports 1 to 4 of the structure of Figure 3. This simulation does indeed show something strange going on at a frequency of around 3.2 GHz.

center to center, over an FR-4 substrate, 9.5 mils thick, with a modeled Er of 4.4.

When a Sonnet EM simulation[3] is run for the structure in Figure 2, and the coupling is measured from port 1 to port 4, as shown in Figure 3, you can see that there is nothing strange going on in the frequency range of 0-4 GHz. This is our baseline coupling that we will compare to later on.

Adding a copper pour to Figure 2 results in the new structure in Figure 4. The copper pour has a realistic spacing of 10 mils to the aggressor and victim traces and therefore has a minimal effect on the 50-ohm impedance of these traces.

Simulating the coupling of the traces and copper pour shown in Figure 4 results in the new coupling plot of Figure 5. The first response to seeing this is sure to be, "It's true. The isolation is worse with a copper pour." Perhaps, and perhaps not. It's all in understanding what is going on, because poorly placed copper will ruin any design, at any frequency from DC to light, as we shall see.

Antenna Basics

To understand what is going on with Figures 4, 5, and 6, we need to understand something about resonances and how antennas work. You may well have heard of a "half-wavelength" antenna. This is an antenna that is one-half of a wavelength long which has good efficiency as a radiator. There are also quarter-wavelength antennas, simply one-half of a half-wavelength antenna placed perpendicular to a perfectly conductive ground. Anything shorter will not radiate well at all without added matching.

If you put a trace or any copper structure

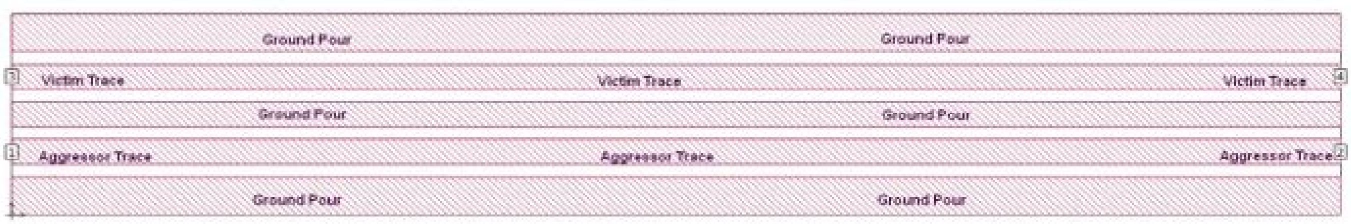


Figure 4: Adding a copper ground pour with a 10-mil gap to the aggressor and victim traces of Figure 2 results in this new structure.

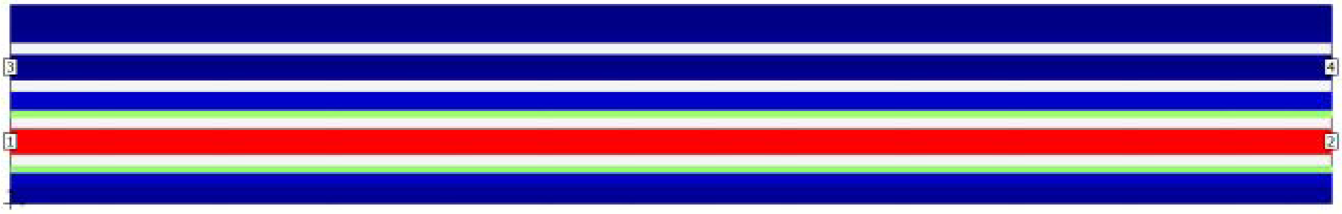


Figure 6a: It is interesting to look at the resulting current densities of the model in Figure 4 when excited. In this plot at 100 MHz there are no resonances present. As can be seen, all the high current is in the aggressor trace and along the edges of the copper pour as would be expected. Red is high-current density while blue is the lower-current density.

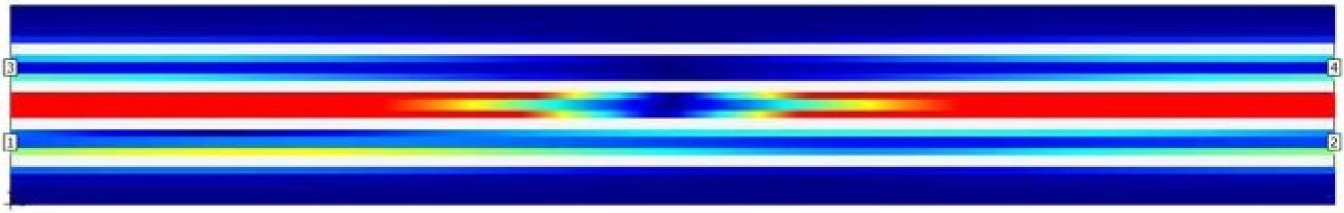


Figure 6b: At a frequency of 3.2 GHz, the resonance can clearly be seen. The victim trace has picked up a lot of current and that copper pour between the traces that we may have assumed was ground is anything but ground now. As can be seen, there is more current flowing in our pour than the signal traces themselves! Red is high-current density while blue is the lower-current density.

on a PCB that is a quarter or half or multiples of a quarter wavelength, they too can be resonant and exhibit very good radiation at specific frequencies, and at every quarter wavelength above that: half, three-quarters, full wavelength, etc.

This is what we see in Figures 4, 5, and 6. We may have assumed that the copper pours are ground, and they are at DC and low frequencies. However, at a sufficiently high frequency, they will resonate as has been shown in Figures 5 and 6. What we have unwittingly made with the structure of Figure 3 is an edge-coupled bandpass filter[4], not a trace shield.

Rules of Thumb

A common rule of thumb is that a signal propagates on a typical FR-4 type PCB at about half the speed of free space[5]. Hence a wavelength at a given frequency is given as Equation 1.

Equation 1

$$\lambda = \frac{Vp}{f} \text{ or } \frac{6.4\,ns/inch}{f\,GHz} = \lambda \text{ inches}$$

Where λ is the full wavelength in inches. Rearranging the equation above to give us the critical, quarter wavelength frequency terms of frequency and length results in Equation 2.

Equation 2

$$1/4\,Wave\,Length \text{ inches} = \frac{1.6\,nS/Inch}{f\,GHz}$$

And re-arranging again, as a function of length,

Equation 3

$$f \text{ GHz} = \frac{1.6\,nS/Inch}{1/4\,Wave\,Length \text{ inches}}$$

For example, knowing that the copper pours in Figure 4 are 1 inch long, Equation 2 predicts that the quarter wavelength frequency is 1.6/1 = 1.6 GHz and the half wavelength is 3.2 GHz, which is exactly where we see the peak resonance of our Sonnet simulation in Figure 5.

The upper equation above can predict the critical trace length based on the frequency of operation. For example, if a trace is carrying a

100 MHz SPI clock, we know that the rule of thumb is that a square wave needs at least five harmonics to accurately reproduce the square wave shape. The quarter wavelength length would then be approximately: 1.6/0.5 = 3.2 inches. Any trace less than about 3.2 inches carrying this clock will have poor efficiency as a radiator.

Another common rule of thumb is if you don't have a repetitive clock signal but instead have a fast rise-time signal. The bandwidth of a known rise-time is shown in Equation 4.

Equation 4

$$f \text{ GHz} = \frac{0.35}{Tr \text{ nSec}}$$

Where Tr is the rise time of the pulse in nanoseconds and f is the equivalent bandwidth of the signal in GHz. It is well known that a 1 ns rise time is approximately equivalent to a 0.35 GHz (or 350 MHz) signal bandwidth.

Given these rules of thumb, we can calculate the critical trace lengths in terms of frequency and rise time of our signals. Normally all our logic edges are quite fast now, faster than they need to be for most clock signals, so I normally use the rise-time equation to figure the required bandwidth and then use that to calculate the critical trace lengths to watch out for.

This "less than a quarter wavelength" rule of thumb applies to all sorts of analysis situations and is a useful thing to keep in mind during the design, and perhaps more importantly, troubleshooting of higher-frequency PCBs[6].

The Fix

Now that we understand what the critical frequencies and lengths are we can move on with our simulations and solutions.

We have just proven that any copper structure, trace, pour, or ground plane can and will act as a resonant antenna if its length gets to or exceeds a quarter or half wavelength of the excitation frequency.

Now, look back to the very first picture of a CPWG layout in Figure 1. Notice anything in those copper pours? Can you see the little vias all along the periphery of the copper pours? I didn't put those there just because I wanted to make life miserable for my PCB fabricator. Actually, those vias stitch the grounds together and effectively provide a way to shorten the length of the copper pours to be less than a quarter wavelength.

How can we fix Figure 4 then? How about effectively making the copper pour in Figure 4 smaller in any direction less than a quarter wavelength? If we place ground stitching vias in the copper pours we can achieve this, as shown in Figure 7.

The addition of properly spaced stitching vias in the copper pour shows that at any frequency, now, the central copper pour acts like a ground and never gets hot as it did in Figures 5 and 6, even at the highest frequency of this sweep (Figure 8).

When properly done, copper pour is indeed acting as the true shielding ground plane that we had envisioned it would be when we put

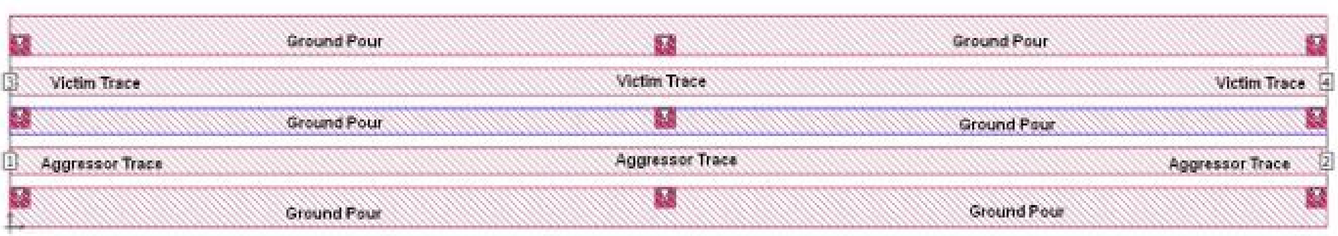


Figure 7: To fix that hot central copper pour we can apply stitching vias to the ground return layer and effectively make the copper pours appear electrically shorter at high frequencies and make them appear more like the ground they were supposed to be in the first place. Here I placed the vias (dark red squares) symmetrically at a distance of 0.5 inches to divide the central copper pour into sections less than the quarter wavelength at 3.2 GHz.

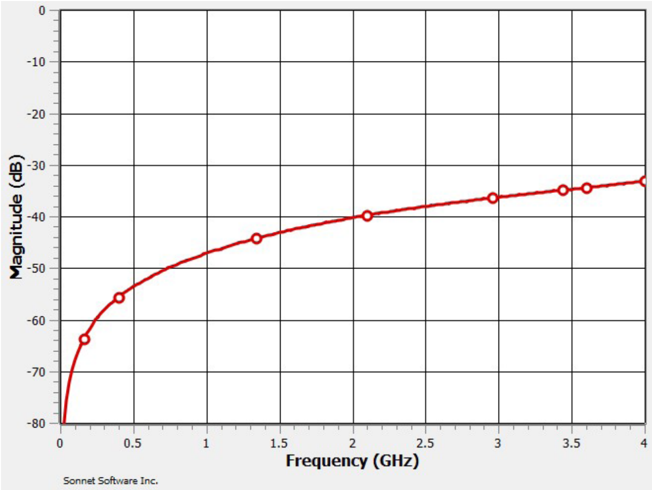


Figure 8: Simulating our structure of Figure 7 with the addition of stitching vias placed in the copper pours shows the resonances are now completely gone.

it there, and it is not making the isolation from the aggressor to the victim trace worse. Comparing the isolation curve of the original model simulation (Figure 3) with our properly stitched ground pour (Figure 8) shows that the added isolation of adding a properly grounded copper pour is about 8 dB in this simulation as shown in Figure 9. Certainly,

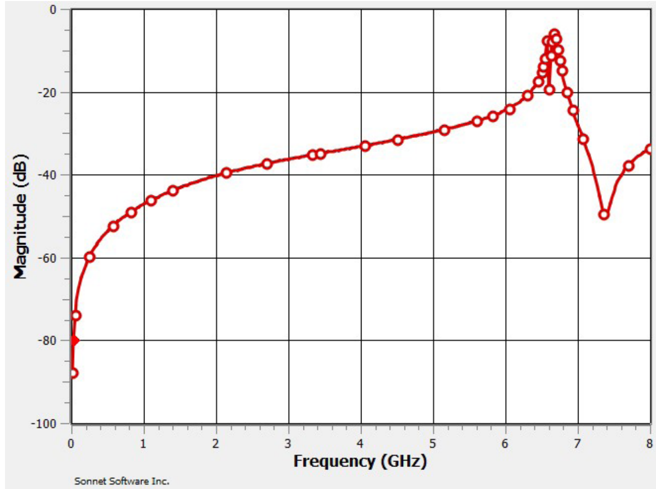


Figure 10: Now, it is predicted that the properly stitched copper pours of Figure 7 will have a new resonance peak at around 6 GHz and that is exactly what we find. We can either place the stitching vias closer together or know that these simulations are done with lossless materials and any real FR-4 PCB will start to have significant losses above 3 GHz, which will be much less of an energetic peak than simulated here.

to me, adding properly done copper pours to all my layers is worth doing for the improved isolation and the improved EM radiation performance of the PCB.

You might now ask: "Since the stitching vias are at 0.5 inch spacing in this example, won't there be a new resonance at 6 GHz now?" And you would be right; extending the sweep frequency of the structure of Figure 7 up to 8 GHz does indeed show a new resonance at 6 GHz, just as we predicted (Figure 10).

We can continue pushing the undesired resonance frequency up by decreasing the space between the stitching vias, and this is one of the reasons I use the less than quarter wavelength as the rule of thumb on spacing in the first place, as it gives plenty of

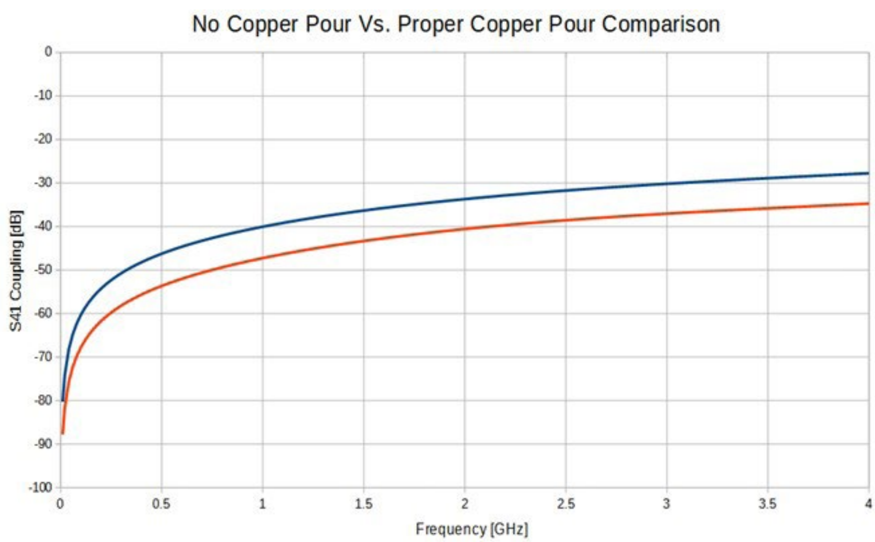


Figure 9: Comparing the isolation curve of the original model simulation (blue curve) with our stitched ground pour (orange curve) shows that the added isolation of adding a properly grounded copper pour is about 8 dB in this simulation as shown. This is proof that properly done, adding ground pours to signal layers does indeed improve signal-to-signal isolation.

margin in the final design. Remember also that these simulations are modeled with lossless copper and substrate material. Any real FR-4 PCB will start to have significant losses by 3 GHz, and these losses always help by lowering the peak currents and undesired coupling at very high frequencies.

Application

As we have seen, every copper structure on the PCB must be less than a half a wavelength, and preferably less than a quarter wavelength, for the highest frequency at which the structures will be excited[6].

Here is how I apply the "less than a quarter wavelength" rule of thumb when I start laying out a PCB. I calculate what a quarter wavelength is for the highest frequency signal on my PCB, and I make a note of that. If I strategically place my vias at a distance less than this around my high-frequency copper pours I will be fine, and there will be some places where I can't maintain this spacing because of other routing requirements, and that's okay. In those places, you can skip one of the vias or place them as best you can at slightly larger distances and the PCB will still work. You can see this in Figure 11 where some vias appear missing because I had to dodge other traces on other layers; your design will still work.

You probably can't tell your PCB software tool that there is a constraint of a via every "X inches," but at the end of the design, you can set the visible grid to whatever you calculated as the appropriate spacing and make sure that the grid is displayed and very bright. This will give you visual cues as to how you did placing the vias and where you may need to squeeze in more.

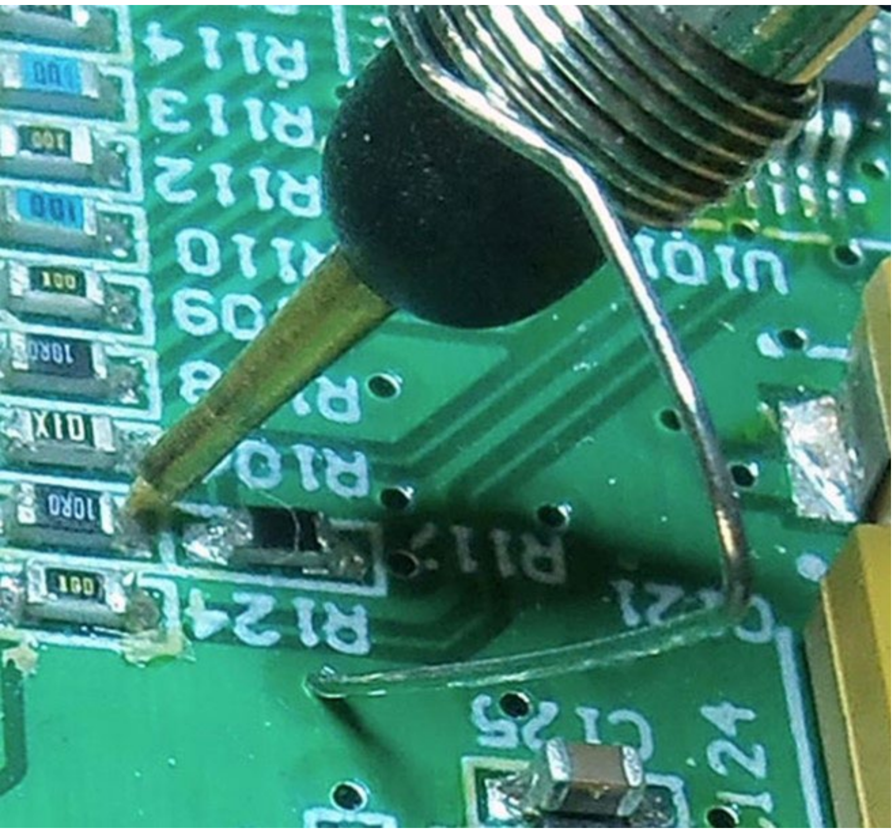


Figure 11: Having a ground pour on the outer signal layers helps when probing high-frequency signals; it is quite easy to place the scope probe ground spring into a nearby stitching via to make the ground contact. Even "slapping on" resistors and capacitors to fix design issues is easier when you have copper pours on the outer layers, and honestly: Who hasn't had to add a part to fix a prototype now and again?

A final note on stitching via hole sizes: If you look at some of the pictures of evaluation boards on the internet[2], you will see that a lot of the time very large holes are used for the stitching vias. This is because, in an X/Y view from the plane of the PCB traces, a large hole has a large copper width in the X and Y directions of the PCB.

This large hole effectively makes a wall-like structure, instead of the "stake" that a smaller hole would produce, and it makes the stitching more effective at higher frequencies with a smaller number of drill holes needed. While using a large hole has advantages on a simple evaluation board, these large holes also block the routing channels needed for more complex PCBs. I usually use my design's minimum hole size for my stitching vias to keep my routing options open, and it works just fine.

Other Benefits

There are other benefits to having a convenient ground on the outside signal layers.

- **Scope probing:** Having ground available helps when probing with an oscilloscope as shown in Figure 11. This is especially true when probing any clock signal where you simply cannot use the long flying lead of the scope probe.
- **Fixing errors:** Well, who hasn't designed a circuit that needed a resistor or capacitor "slapped" onto it to get it to work properly? Having a ground nearby on the top and bottom layers makes this trivially easy.
- **Improved radiation performance:** A properly placed copper pour on the signal layers does indeed reduce the radiation of the design in general by bending the electric field lines into the copper pour and not letting them be so far out into space. Think about it this way: If I create an antenna trace on a PCB and then I surround it with copper pours on just the sides, I will have made a sort of coaxial structure, and I have ruined that trace's effectiveness as a radiator because I have shorted out the electric field from the surrounding air. Everyone can probably reason that a coax cable is the best way to transfer signals without radiation, right? A properly designed copper pour does nearly the same thing to nearby traces. Note that you may have to adjust the final trace width to maintain the desired impedance levels with a close copper pour[7].
- **Heatsinking:** More copper means better heat sinking in general for the PCB as a whole, and the stitching vias thermally tie it all together.

Possible Downsides of Adding Copper Pours

There may also be disadvantages to this approach.

- The possible increased cost of adding vias and then having to drill them
- Takes time to add copper pours and the stitching vias correctly
- Incorrectly done copper pours may indeed make the situation worse

Conclusion

It isn't a matter of, "Copper pours on a signal layer make things worse." It's more like, "Poorly placed copper anywhere will ruin any design." Once you understand what is really going on, with the help of easy-to-use EM simulation tools, you will improve your designs immensely. DESIGN007

References

1. "How to Make a Quick Turn PCB That Modern RF Parts Will Actually Fit On," and "Benefits of Coplanar Waveguide Over Ground," by Steve Hageman.
2. For more examples of boards created with CPWG construction, just do a web image search for "Hittite Evaluation Board." Hittite (now part of Analog Devices) is famous for doing all their prototype boards using the CPWG technique.
3. The Sonnet EM simulator and a free lite version are available at www.sonnetsoftware.com.
4. To see examples of filters of this type, do an internet image search for edge-coupled filters.
5. "Propagation Times and Critical Length—How They Interrelate," by Douglas Brooks.
6. Another example of using the "quarter of a wavelength" rule of thumb, visit AnalogHome: Decoupling RF Circuits - Part 1.
7. There are numerous free calculators available that will do calculations for CPWG structures, or you can use Sonnet.

Steve Hageman is the founder and lead engineer at Analog Home.

Six Key Considerations for Designers New to PCB Layout

Connect the Dots

by **Matt Stevenson**, SUNSTONE CIRCUITS

Demand continues to increase for boards used in consumer electronics, intelligent machines used in manufacturing, and smart devices for health services applications. Our industry needs more smart people designing PCBs to help drive artificial intelligence (AI) initiatives and power the Internet of Things (IoT), which is why we are welcoming new designers into the fold every day.

The PCB layout process is, at its core, a seemingly simple one—connect all the points of the components to their necessary endpoints. In practice, it can get complicated in a hurry. For those new to design, it's important to recognize there is much more to it than just routing traces from point A to point B.

So, what are the important design considerations you should be sure to consider?

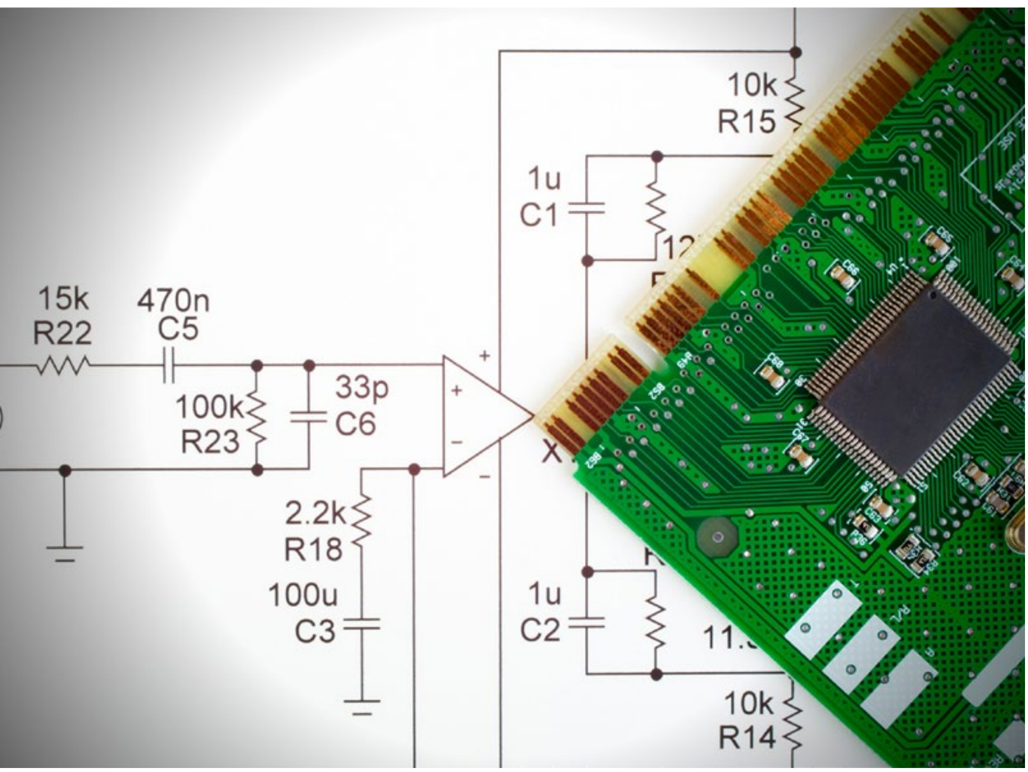
The following are six design considerations to help ensure your design is reliable, includes all the necessary connections, is optimized for manufacturability, and dissipates heat away from the electronics.

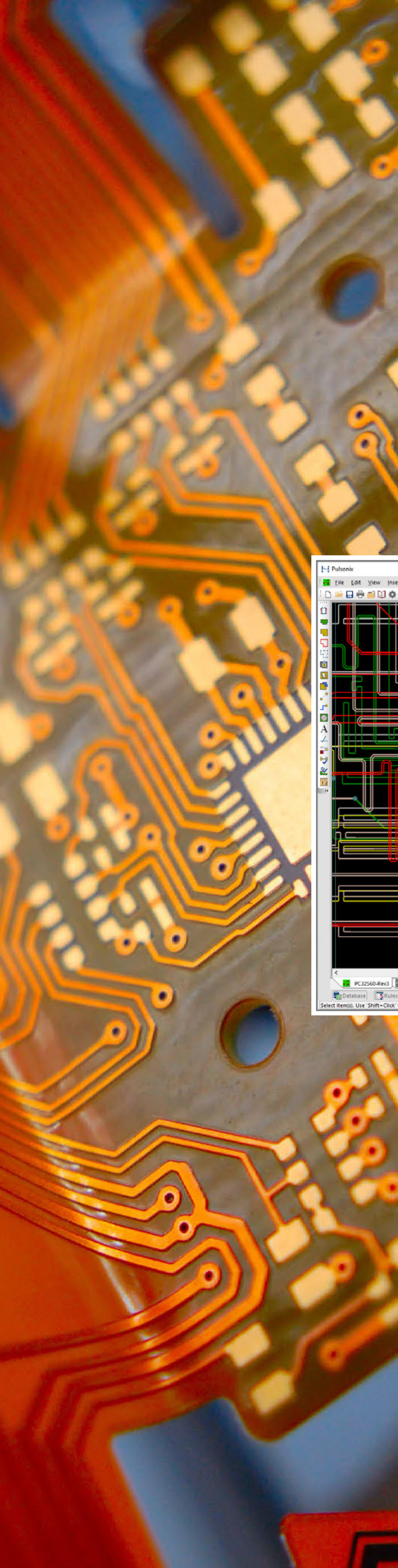
1. Separation

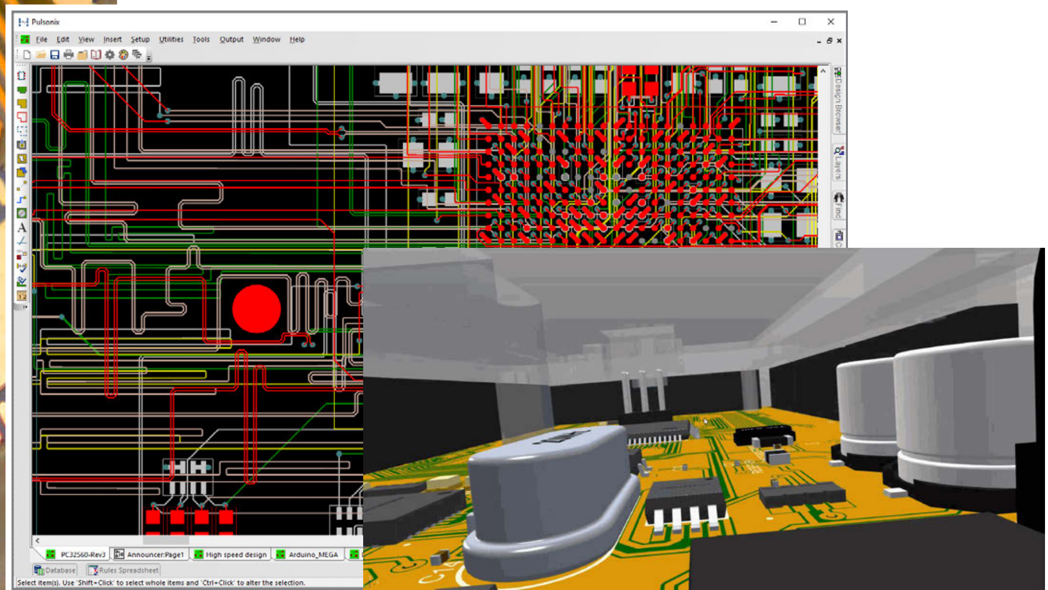
In most design applications, it's important to maintain separation of signal types. The most common example is keeping analog and digital signals and their associated grounds separate. A good design technique for keeping signals separate involves grouping the sections of the schematic—digital and analog that share a common ground—together in proximity and then placing the ground plane directly below this grouping. Similarly, running only analog lines over or under the analog ground layer will help reduce capacitive coupling of signals.

2. Four Tips in One for Minimizing EMI

Electromagnetic interference (EMI) can really mess with board performance. EMI is a disturbance created by electromagnetic induction and







electrostatic coupling or conduction. Here are four tips for reducing EMI from your design:

1. Choose surface mount device (SMD) components over through-hole parts. Generally, the leads on the through-hole parts create higher levels of inductance and thus an opportunity to create EMI.
2. Design with multilayers, adding a ground plane on the layer directly below the external signals (2 and n-1). The presence of these planes near the signal will effectively reduce the return path, keep signals clean, and reduce EMI emission. Connecting decoupling or bypass capacitors to these planes offers another effective technique for reducing EMI because you are creating short and logical return paths.
3. Limit the operating current and/or the rise times of the signals to help reduce larger fluctuations in current. This creates lower EMI emission rates.
4. Match the impedance on signals. This is a critical design practice, especially at higher signal speeds that will reduce the opportunity for signal reflection, harmonics, ringing, and overshooting digital signals, all of which increase the EMI radiation.

3. Manage Heat

If not properly managed and mitigated in the design phase, heat can diminish board performance and durability. Most electronic components generate heat during use. Most have some tolerance threshold beyond which they can fail.

To manage heat effectively, identify which components generate the most heat in your design. You should distance them from other heat generators and any heat-sensitive components during layout. Use design components such as heat sinks, cooling fans, or thermal vias to remove the excess heat from the board. If you are unsure of heat tolerances, the information on heat generation and sensitivity to heat can usually be found on the component datasheets.

4. Component Placement

After considering functionality, signal separation, EMI, and heat, it's time to place components on your layout. Here are several important placement considerations:

- Seek to optimize component placements from a design integrity standpoint and increase the assembly yields.
- Shorten the distance of the trace runs as much as possible. This results in less signal loss, faster speeds, and a cleaner overall signal.
- Orient parts in a similar fashion and perpendicular to at least one edge of the PCB if possible and consider the height and width of components.
- When it is feasible, use a stair-step approach to placement to avoid trapping a short component between two taller components.
- If you can, place all SMD components on one side of the PCB unless you really need to use both sides.
- Place all through-hole components on the top side.

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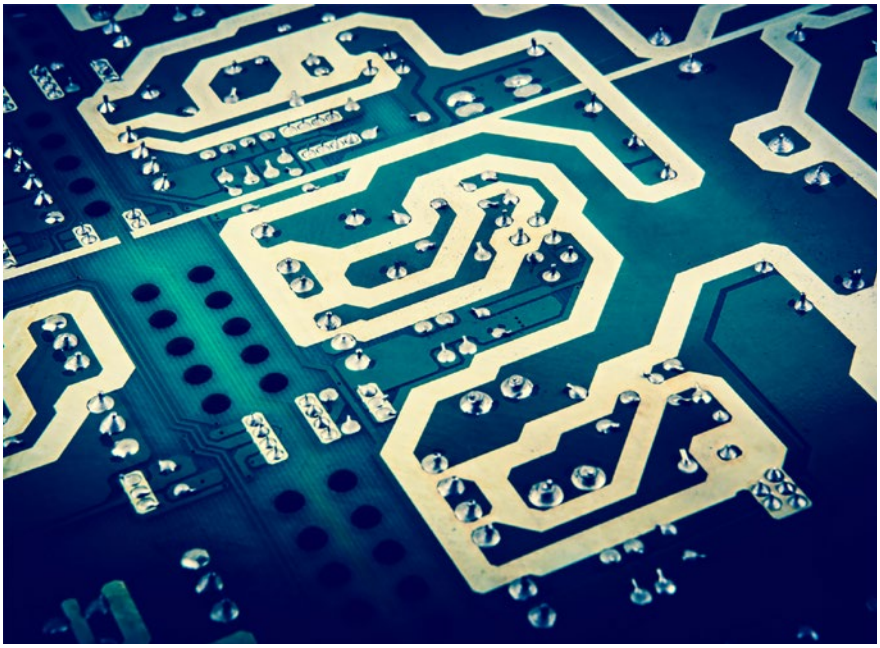
[1] IPC. (2017). Findings on the Skills Gap in U.S. Electronics Manufacturing.



5. Power Delivery

Develop a plan for delivery of power to all the necessary parts. It is a good practice to draw power from a plane or a bus. You never want to simply run the power from one component to the next, as that practice can really cause lots of issues with your designs. Also, make sure to use bypass capacitors and low pass filters to ensure that there are no unwanted spikes or outages to critical components.

6. Verify Components' Footprints

Measure twice, cut once.

You should verify—either on your own or through a library process—that the electronic versions of all components match the physical. Rely on your datasheet during this process to verify that the pad size and pitch are what is documented. The datasheet is also your best tool to confirm that hole size in the footprint not only matches but also considers maximum material condition. Everything has a tolerance so use the worst case for establishing the maximum material condition. There is nothing worse than receiving your boards from the manufacturer and thinking you are ready for assembly, then realizing that either the part in your hand will not fit onto the spot on the board or that the leads for the part will not fit into the hole.

PCB layout isn't as easy as it might seem. By following a logical process and planning for the inevitable you can increase the likelihood that your prototype will come out as you had designed. **DESIGN007**

Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, click here.

DFM 101: Edge Plating

Article by Anaya Vardya
AMERICAN STANDARD CIRCUITS

Introduction

One of the biggest challenges facing PCB designers is not understanding the cost drivers in the PCB manufacturing process. This article is the latest in a series that will discuss these cost drivers (from the PCB manufacturer's perspective) and the design decisions that will impact product reliability.

What is Edge Plating?

Edge plating is the encapsulation of the edges of printed circuit boards to improve EMI shielding of higher frequency designs, as well as for improving chassis ground in systems. The requirement for edge plating is being implemented for single axis, as well as multiple axis edges of the circuit board, including all four edges.

Edge plating is created when a rout path is implemented prior to the metallization of the circuitry features of the printed circuit board and is sometimes referred to as "plated rout." The design requirements for implementing this technology are dependent on the requirement for the number of edges of each board, the size of the board, and whether the boards will be delivered in a multi-up array.

Stability of the material used for manufacturing of the board will also play a part in the development of the routing requirements. Materials where the reinforcement is not the standard glass-reinforced FR-4 type may require an alternative routing design to improve the structure of the parts inside the panel that is used to carry the parts during manufacturing. The parts are processed still intact inside the carrier panel, also called an array, used for manufacturing and assembly, requiring the develop-

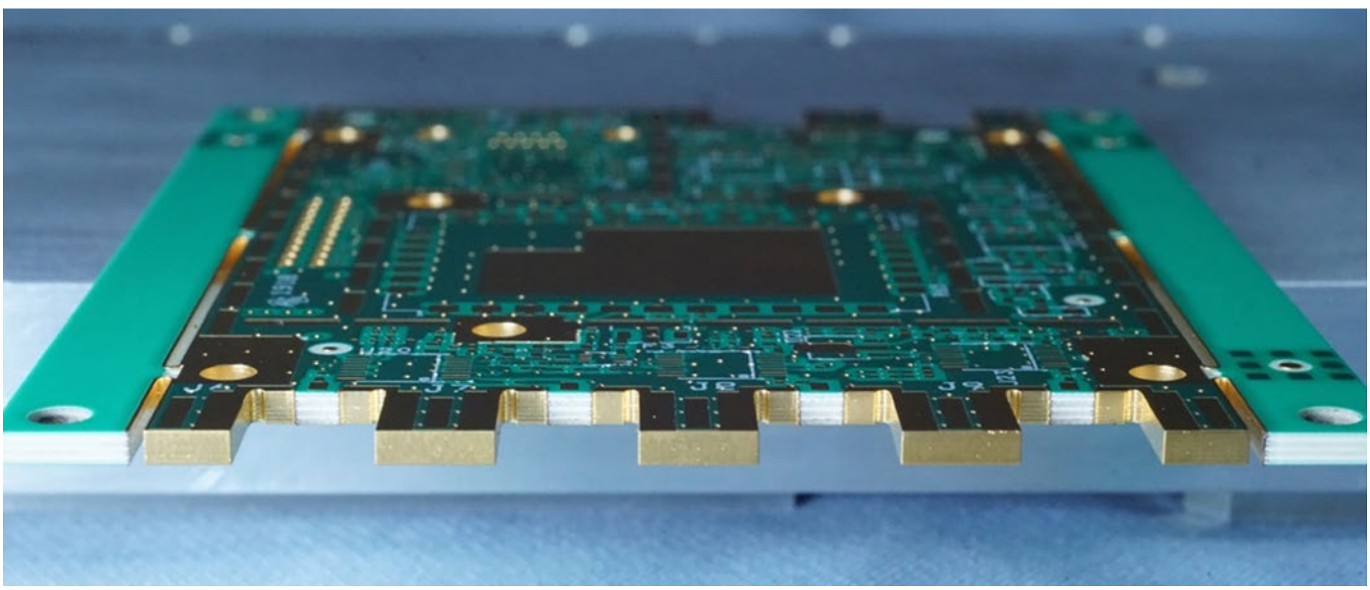


Figure 1: An example of edge plating.

ment of tabs in some cases for edge plating. For a single edge requiring plating, tabs may not be required for stability.

Development of Tabs for Transporting the Panels

The drawing on the left in Figure 2 shows how perforated tabs are implemented for a circuit that is manufactured in a multiple-up array. The requirement is that the tabs being used to hold the board in the array will be broken off after the assembly operation (also called singulation). Figure 2 (right) shows a solid tab that is placed at the plated rout process. In both cases the internal and external layer artwork around the tabs must be void of metal. This will prevent the metal from being exposed in the singulation process. When a solid tab is used, the tab is removed at the final fabrication stage using a router (the same router that removes standard parts from the carrier panels). Removal of the tab will leave a small protrusion along the edge of the part.

Also detailed are the minimum requirements for the dimensions of the tabs. Placement of the tabs is based on assembly requirements and materials being used to construct the circuits. Less dimensionally stable materials, typically non-reinforced materials, as well as thin (<0.060") and thicker panels (>0.200"), will require additional tabs for stability in processing. Conservatively, the tabs are placed every two inches along the plated edges. For non-FR-4 materials this is more the rule.

Design Rules for Plated Edges

It is required that the plating not only encapsulate the edge of the panel, but that the plating also wrap around to the surface of the panel. This is shown in Figure 3, and the minimum distance the plating is required to wrap around to the surface is 0.015". The wrap-around is required for internal processing and adhesion of the plating to the edge. Also detailed is the minimum distance a feature can be placed to the wrap around plating (0.010") as well as the distance required for an adjacent routed feature (0.100").

It is typical that the plating be continuous along the entire edge of the circuit, but interruptions in the plating can be designed with two methods. By placing a tab at the interruption, and subsequently removing it, the tab prevents the plating (Figure 4a). Alternatively, the plating interruptions can be removed at the final routing stages. The subsequent removal of the plating will leave a small tab or an indentation into the circuit (Figure 4b). The inden-

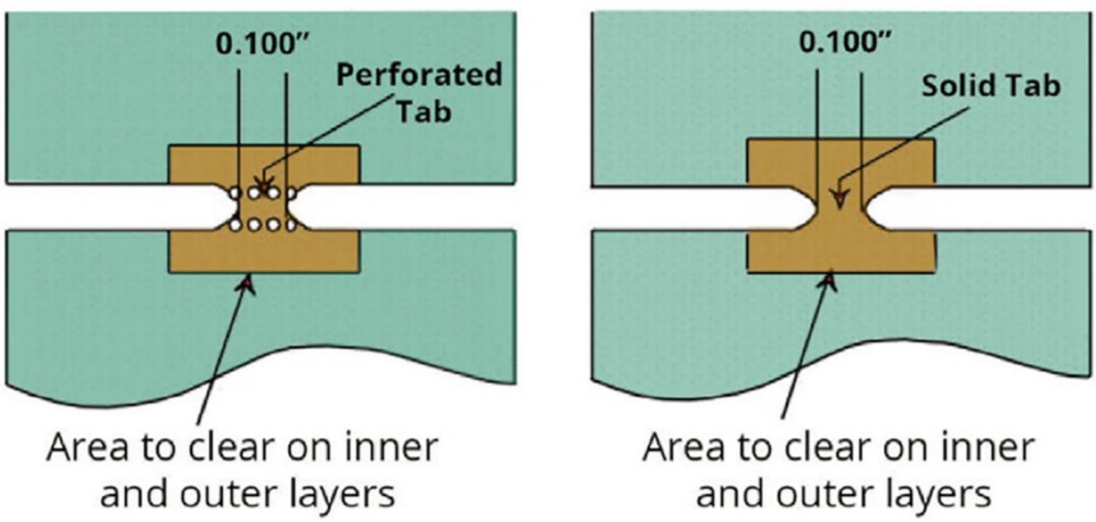


Figure 2: A solid tab that is placed at the plated rout process. In both cases the internal and external layer artwork around the tabs must be void of metal.

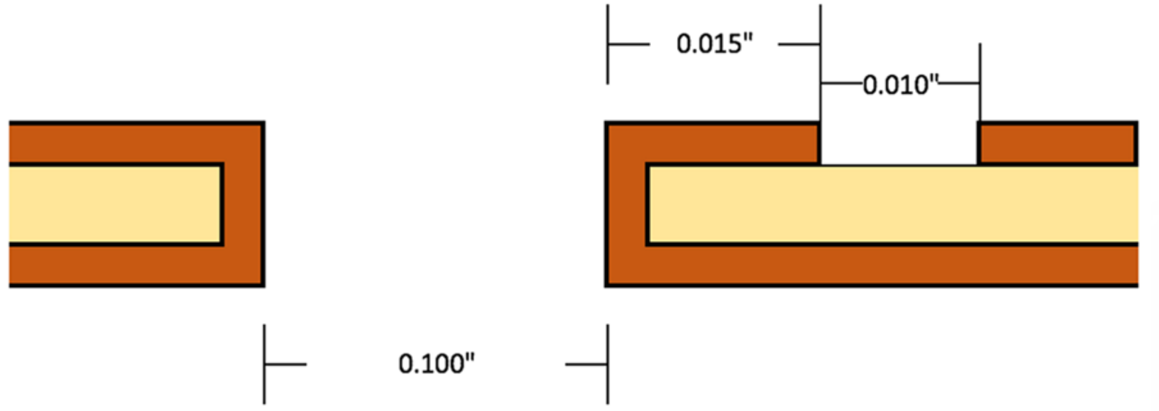


Figure 3: It is required that the plating not only encapsulate the edge of the panel, but that the plating also wrap around to the surface of the panel.

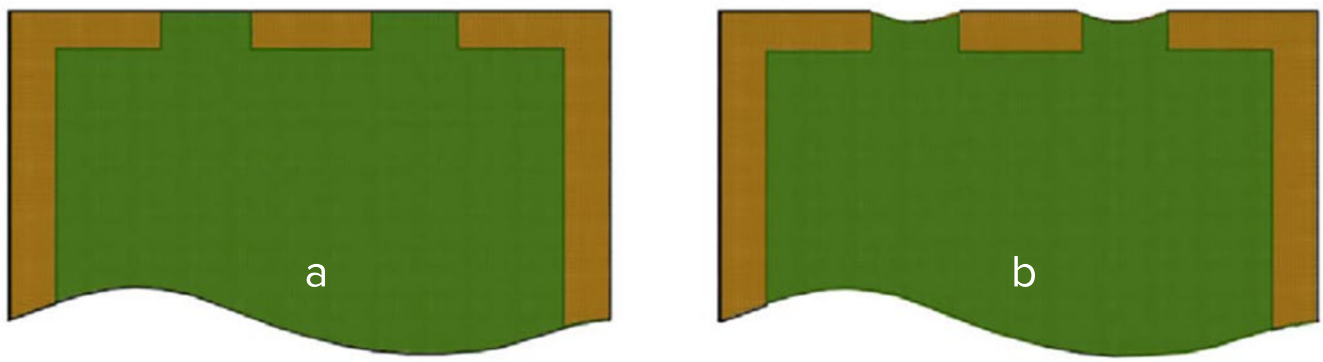


Figure 4: a) By placing a tab at the interruption, and subsequently removing it, the tab prevents the plating; b) the subsequent removal of the plating will leave a small tab or an indentation into the circuit.

tation is created when the router bit contacts the edge where the plating is removed and advances into the circuit to completely remove the plating. When the interruption of the plating is a minimum of 0.200" the use of a tab to prevent the continuous plating can be used. When less than 0.200" the edge will be plated entirely across and subsequently removed by the routing process described.

Edge plating typically involves the connection of one or more of the internal planes in a board. These planes extend to the edge of the board and are electrically connected by the plating process. Those layers are typically fabricated with a polarity border (ref. 0.050") to prevent exposed copper when they are routed and removed from a panel.

Understanding the cost drivers in PCB fabrication and early engagement between the designer and the fabricator are crucial elements that lead to cost-effective design success. Following your fabricator's DFM guidelines is the first place to start. **DESIGN007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to… Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals;* and author of *Thermal Management: A Fabricator's Perspective*. Visit I-007eBooks.com to download these and other free, educational titles. He also co-authored "Fundamentals of Printed Circuit Board Technologies" and provides a discussion of flex and rigid flex PCBs at RealTime with… American Standard Circuits.

MilAero007 Highlights

The Government Circuit: Ready to Tackle 2022 ▶

As anticipated, it was a busy close to 2021 in Washington, and we saw resolutions on several major legislative priorities, including the annual defense authorization bill, which affects billions in future defense electronics spending. Meanwhile, negotiations on the U.S. Innovation and Competitiveness Act (USICA) remain on the back burner but could heat up in Q1. Read on for some of the recent highlights from 2021 and a look forward to 2022.

Real Time with... IPC APEX EXPO: Advocacy in Washington ▶

Editor Nolan Johnson sits down for an interview with Chris Mitchell, vice president of Global Government Relations at IPC. They discuss the industry's advocacy in Washington to educate Congress on our key issues, as well as the growth in global advocacy by IPC.

Calumet Electronics Receives 'World-class Team' Award from Northrop Grumman ▶

Calumet Electronics Corporation received a World-class Team award from Northrop Grumman Corporation for its outstanding performance. Calumet is one of just 24 small business suppliers across the nation to receive the award and the only recipient from Michigan.

Real Time with... IPC APEX EXPO: Update From PCBAA ▶

PCBAA Chairman Travis Kelly sits down with Nolan Johnson to discuss the new association's recent activities and plans for the future. The Printed Circuit Board Association of America is focused on advocating for manufacturing in America.

Ventec's USA Facility Receives AS9100-D & ISO 9001:2015 Quality Certification ▶

Ventec International Group is pleased to announce that its U.S. facility in Fullerton, California, is now certified according to AS9100 Revision D and ISO 9001:2015, the quality-management standard for the aviation, space, and defense industries.

Lockheed Martin Aeronautics Adopts Siemens' Xcelerator Portfolio ▶

Lockheed Martin's Aeronautics business has selected Siemens' Xcelerator portfolio of software and services to support its digital engineering transformation.

Collins Aerospace Completes Air Launched Effects Demonstration for U.S. Army Future Vertical Lift Program ▶

Collins Aerospace has successfully demonstrated a ready-now Mission Systems solution to support the operations of Air Launched Effects (ALE) from Army Aviation's Enduring and Future Vertical Lift (FVL) fleet.

NASA Selects Developer for Rocket to Retrieve First Samples from Mars ▶

NASA has awarded a contract to Lockheed Martin Space (Littleton, Colorado) to build the Mars Ascent Vehicle (MAV), a small, lightweight rocket to launch rock, sediment, and atmospheric samples from the surface of the Red Planet.

Time to Upgrade to Windows 11?

Fein-Lines

by Dan Feinberg, FEIN-LINE ASSOCIATES

My friends, family, and clients have asked me, "Should I upgrade to Windows 11? Is now a good time?"

If you're like most PCB designers, you are using Windows 10 for everything you do. It's true that Windows continues to be the dominant operating global system, with all versions of Windows comprising slightly over 70% of the global market share for desktops and laptops of all types and brands. For mobile phones, however, Android dominates.

Figure 1: A Windows 11 desktop.

Windows 10 has the largest piece of that computer pie, but Windows 11 is starting to gain share rapidly. In just a few months, Windows 11 has gained a significant share of the personal computer market. The rapid growth of Windows 11 is probably due to the push from Microsoft to most Window 10 users. Apple's MacOS and iOS rank second, mainly due to the popularity of the iPad. Linux maintains a small but stable share, primarily due to its popularity with users who prefer open-

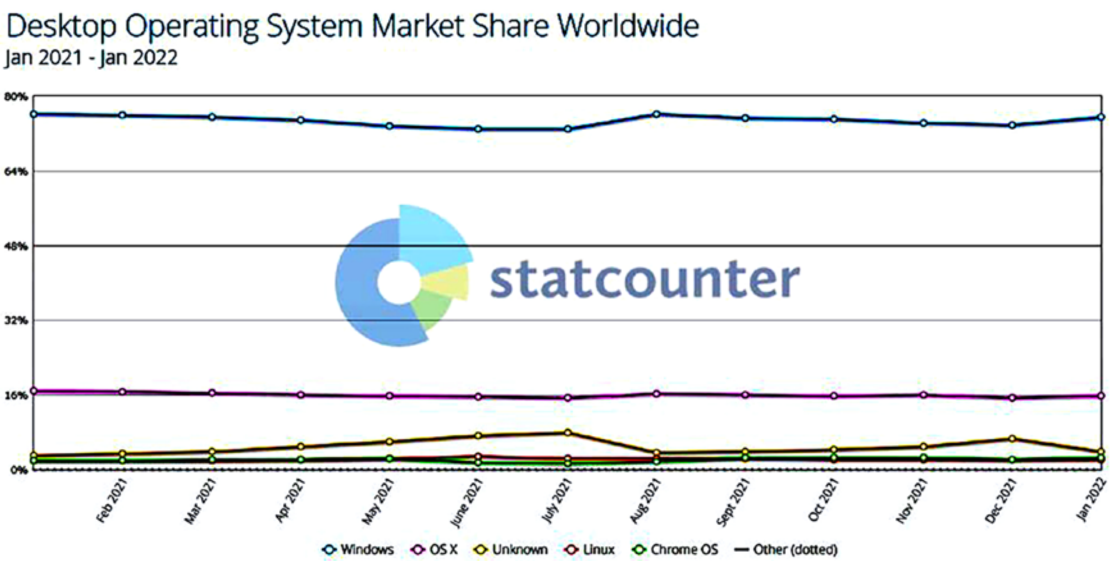


Figure 2: The global OS market share. Windows is the overwhelming favorite.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source software and intend to avoid the influence of major OS developers.

In fact, it was just about time for a new version of Windows as it has been over five years since Windows 10 was introduced.

Microsoft has detailed several new features for Windows 11, including:

1. An easy way to stay in touch. With Chat in Microsoft Teams, you can connect to friends and family from your PC regardless of what computer, phone, or tablet they are using— PC, Android, iOS, or Mac. Chat is built right into the Windows taskbar; you can use Microsoft Teams to connect for free via video and phone calls or chat—no need to look at your phone. If you prefer to use a real keyboard to text, then Windows 11 makes connecting really easy.

2. Intuitive navigation and easy organization. With Windows 11, the user experience has been simplified. It's a clean, fresh design that is new, yet immediately familiar. The "front and center" placement of icons makes searching for anything a streamlined and intuitive affair. I did not like it at first just because it was different, but now I find it quick, simple, and easy to get used to.

3. Bring balance to your desktop. You can group and organize open windows and easily pivot between them with the new multi-tasking tool, Snap Assist. Effortless to use—just drag windows to the edge of the screen to activate in just a few clicks.

4. Lots of widgets. Your favorite photos, weather, the world news, stocks, and more. Widgets help you find content that matters to you. Offering you the information you want right at your fingertips, widgets are great ways to get bite-sized moments of news, entertainment, and more throughout your day.

5. Innovative devices and features. There are things you love about your phone and tablet. And these are now provided on your PC. Microsoft has made enhancements to touch, voice, and pen inputs. New Windows devices are more versatile, capable, and easier for you to use—however you want to use them.

Some of my personal favorite features include:

- You can easily keep several windows open and quickly minimize all but the active one.
- The secret additional start menu makes accessing important features like the Command Prompt, the Control Panel, and the Task Manager easier. You can access it two different ways, either by pressing the Windows key + X, or right click the Windows icon/Start button.
- Quickly open pinned programs from the taskbar, find out how much storage space programs and apps are using quickly and easily, Android app support, virtual desktops, and many more. In addition, Windows 11 is compatible with DirectX12 (or later) so if you are a gamer or are looking for maximum graphics quality, that may be important.
- It seems fast even when running multiple monitors and open windows and apps at the same time.

If there are feature locations that you don't like, such as the new centered task bar, it is possible to reset many of them to the old Windows 10 location. Perhaps the most important feature is that because it's new, there will continually be new updates and improvements. It is designed for compatibility with today's multiple e-devices.

Most computers bought or built in the last few years will be compatible with Windows 11. There are some that will tell you that they are not compatible when you try to upgrade,

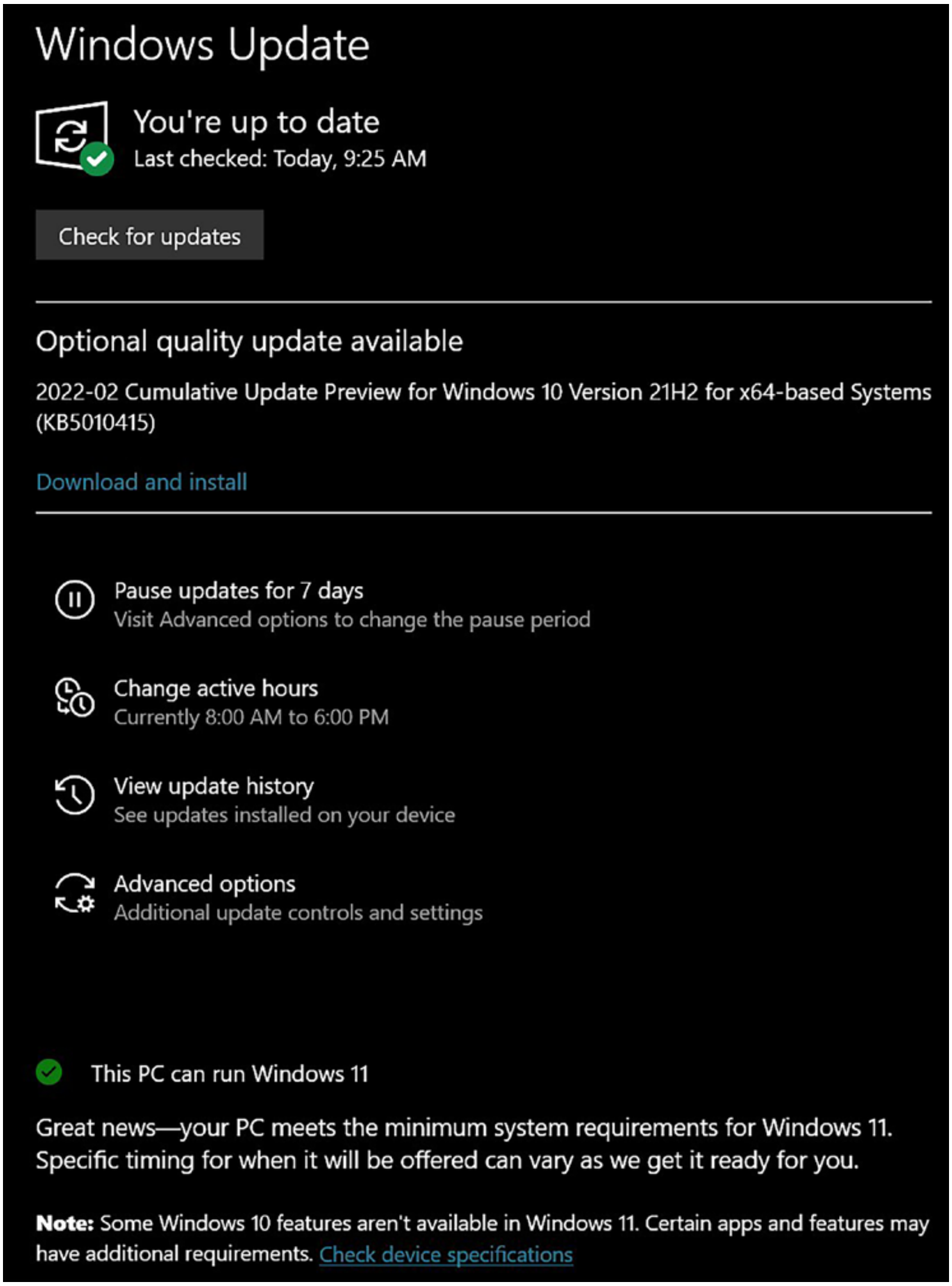


Figure 3: Check to see if your computer is ready to upgrade.

but things such as the amount of RAM needed (4 Gb minimum) or the amount of storage (64 Gb or more) can be upgraded, and some are just settings such as the need for Trusted Platform Module (TPM) to be enabled. Most computers built over the last few years have this ability and allow for TPM to be enabled. However, if your computer is not, or cannot be made compatible with Windows 11, be assured that Windows 10 will continue to be supported for the next few years.

One important feature is that if you are upgrading from a legal copy of Windows 10, getting Windows 11 is free.

So, should you upgrade now? First, go to Settings and check to see if you have Windows 10 updates available. If so, do those first.

If you are comfortable with dealing with some potential glitches, go ahead. I installed Windows 11 on one of my computers over a month ago and while there have been a few minor glitches, I have had no real issues. In fact, the latest update/fix download seems to have fixed the few issues I did have. Windows 11 is now publicly available and, of course, the more that we use it, the more bugs will be discovered and fixed.

Here's my recommendation: If you only have one computer and you are looking for the best possible initial experience, I would wait for the next update. However, I am now much more comfortable recommending that you upgrade than I was just a month ago. By the end of February, Windows 11 grew to over 16% of global market share. **DESIGN007**

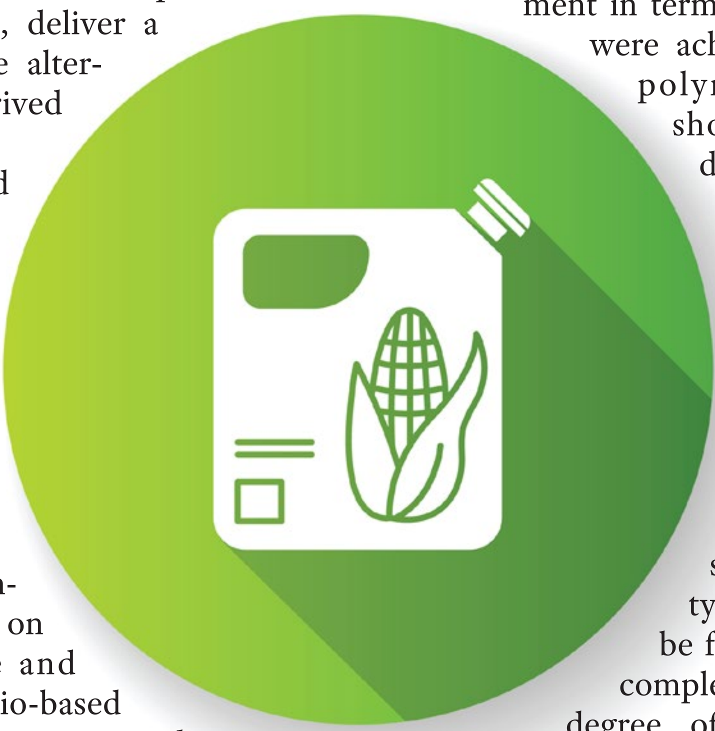
Dan Feinberg is an I-Connect007 technical editor and founder of Fein-Line Associates. To read past columns or contact Feinberg, click here.

What Can Manufacturers Expect From Bio-based Conformal Coatings?

Sensible Design

by Phil Kinner, ELECTROLUBE

Globally, managing finite resources is imperative as we strive to achieve a more innovative and lower emission economy. Reducing dependency on fossil fuels in the chemical industry has led to the emergence of new bio-based alternatives, but what do these bring to the table for electronics manufacturers? Bio-based materials, obtained from biological resources (biomasses, feedstock, plants, and biological waste), deliver a viable and sustainable alternative to materials derived from petrochemicals.



We have developed a new coating incorporating 75% bio-organic content from renewable sources. It's a global first for the industry and is completely free from solvents. It meets the needs of both manufacturers and consumers, essentially based on ethics, performance and process. So, how will bio-based coatings impact performance and what can you expect? Let's explore bio-based coatings in more detail.

1. What are the benefits of bio-based coatings?

First, it goes without saying that bio-coatings have significantly less impact on the environment and meet the ethical needs of manufacturers and end users. However, the most surprising benefit observed during the development of this bio-coating was the improvement in terms of performance that were achieved. The bio-based polymers we developed showed improved condensation resistance, thermal stability, flexibility, and adhesion over many petrochemical-derived polymers that we developed. Nature truly is an amazing source of inspiration.

More or less every single ingredient in a typical formulation can be formulated from either completely bio-based or high degree of bio-containing raw materials, with the current exception of flame retardants. The bio-coating has per-

formance in abundance and top environmental credentials to match, making it a win-win solution. We are also "future-proofing" at the same time; for instance, if the government says to introduce new environmental measures in a couple years' time, then manufacturers are covered.

2. What is the financial impact for a bio-based coating over a traditional chemistry?

Currently, many of the supply chains of these new raw materials are developing scale economies, so the raw materials are more expensive than their mature, petroleum-derived alternatives. Therefore, the improvement in performance of the bio-based coating material, over a more traditional petrochemical material, can come at an increased cost. However, as electric vehicles become more commonly adopted and the internal combustion engine (ICE) becomes more economical and less widely used, oil production is likely to slow and become increasingly expensive, so at some point in the near future, the bio-based materials are likely to become more economical than oil-based feedstock.

3. Which conformal coatings are the most popular and why?

This is a tough question and one we get asked a lot. In general, I would say that acrylic materials and UV-curable materials are amongst the most popular. Acrylic materials remain amongst the most popular class of coating due to their ease of application, rapid drying by solvent evaporation, and ease of re-work—immerse them in solvent, wash with solvent, et voila, no coating remaining. However, acrylic coatings provide less adequate levels of protection in more demanding applications, such as condensation and high environmental impact. Many end users are beginning to realise that they will need to move away from acrylic materials due to both of these factors. Especially prevalent is the requirement of many automotive OEMs to pass a condensation test (e.g. K15-19 from BMW GS95024-3-1). Even in aerospace applications, there is an increased focus on condensation resistance in coated assemblies due to the rapid environmental changes experienced during descent from 40,000 feet to a hot and humid runway, for example.

As for UV-cure materials, the rapid nature of the primary UV cure, as well as the polymerisation process itself, tend to cause significant amounts of shrinkage, which creates a lot of stress in the coating that is commonly alleviated by stress-cracking during thermal cycling. The materials must also contain a secondary curing mechanism to ensure material beneath components, or otherwise shadowed from UV radiation by taller components, develops hardness, and cross-links. This is commonly a moisture-initiated cure reaction and can take weeks, months, or even years to complete, due to the fact that the outside of the material is partly cured from exposure to UV radiation; moisture must permeate through this membrane and CO_2 gas produced during this curing process must permeate back out through the same membrane.

The benefit of a 2K UV-curable material is that once the two components are mixed, the reaction will proceed to completion in less than 24 hours in these shadowed areas that are not exposed to UV radiation. Also, the additional cure nature of the reaction ensures significantly less shrinkage and less stress, resulting in more flexible coatings that can better survive thermal shock.

4. Why did we decide to include bio-content in our conformal coatings and how did we test them?

We are very committed to the ISO 14000 obligations. It is an entirely logical and natural progression to look at how we can reduce the carbon footprint of our materials. The only surprising factor was the degree of performance improvement achieved with these innovative new materials.

Whilst the development focus is very much on meeting the highly demanding requirements of automotive and aerospace applications, the high-performance levels of these materials make them a great choice for any application. The materials really come into their own whenever thermal shock cycling and condensation resistance are the two main failure mechanisms. As for testing the bio-based coating, much of the development work focussed on doing a lot of work in harsh environments, testing and demonstrating improved condensation resistance due to the combined improvements of thickness and coverage provided by the material, further to the usual automotive requirements of thermal shock and max continuous operating temperatures with long term thermal humidity ageing,

5. Are there possibilities to increase the amount of bio-content within a coating and are more bio-based coatings in the pipeline?

There could be opportunities to increase bio-content in coatings but I don't see it as a binary equation. We are developing more bio-based coatings (and bio-based encapsulation resins) so the industry can expect more high-performance, green solutions to come from Electrolube—now part of MacDermid Alpha Electronics Solutions. Having proven what this new product can do in terms of the environmental and performance benefits, we're aiming to include bio-based materials in all our new product developments moving forward.

In years to come, more policies could be introduced to make fossil-fuel counterparts less appropriate and more expensive, perhaps through a carbon tax. Such future incentives would boost the demand for bio-based alternatives across all market segments. I hope you have enjoyed this month's column and learned more about the benefits of bio-based coatings. In my next column, I'll be exploring more conformal coating related topics. DESIGN007

Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch the micro webinar series "Coatings Uncoated!"

Leveraging Model-based Engineering to Manage Risk, Part 2

Digital Transformation

by David Wiens, SIEMENS EDA

In my last column, I highlighted the critical drivers for model-based engineering. I explored the decomposition of system components from the initial requirements (the left side of the V diagram), emphesizing the advantages of maintaining a digital thread during this architectural break downacross multiple domains. In an earlier column, I addressed the role of the digital prototype in a digital transformation. I'd like to draw those two themes together and talk about the right side of the V (integration and verification).

In traditional flows, system verification is all physical. You test individual units—meaning each PCB by itself, each IC by itself. Once these are verified, you put these components together and move on to subsystem verification to make sure the parts perform correctly with each other. Even at the individual board or IC level, the cost of respins is exorbitant, so waiting until they're all integrated (including mechanical structures and software) sends the cost and schedule through the roof.

A better approach leverages digital twins to shift verification to earlier in the flow by replacing physical prototypes with digital models. In this process, digital twins, as opposed to physical prototypes, are progressively integrated and verified—from the individual units all the way to the complete system.

Note that there are two ways to leverage digital twins:

1. Analysis (often during decomposition and design) to consider trade-offs and optimize a design (ideally automated and leveraging artificial intelligence).
2. Verification to ensure compliance against a requirement or derived design rule.

As a design progresses down the left side of the V (from high-level requirements through systems-level architectures to component-level implementations), the digital models increase in fidelity (from very abstract to very realistic). Likewise, as a product progresses from high-level requirements (top left) to system-level validation (top right), the model of the integrated system increases in fidelity.

To ensure errors are found and fixed as soon as possible, verification must be done continuously—from concept to production. The challenge is to leverage the appropriate level of model fidelity at the right time. Just because you have the most accurate model possible doesn't mean you can do anything with it. For example, simulating every signal on a board is compute-intensive—imagine doing that across a system-of-systems, simultaneously considering multiple disciplines like signal, power, thermal, and structural integrity. While highly abstract models are the only thing that exist in early architecture decomposition, they actually prove more valuable when considering system-level trade-offs across multiple domains at any point in the design process.

Some higher-level requirements can be verified at only the lower levels because they necessitate some white box testing (using detailed models of the inner workings). This makes a bottom-up flow essential, in which you start with the lowest level models and work your way up by merging them together—verify the components, then assemblies, then subsystems, then systems, and even systems-

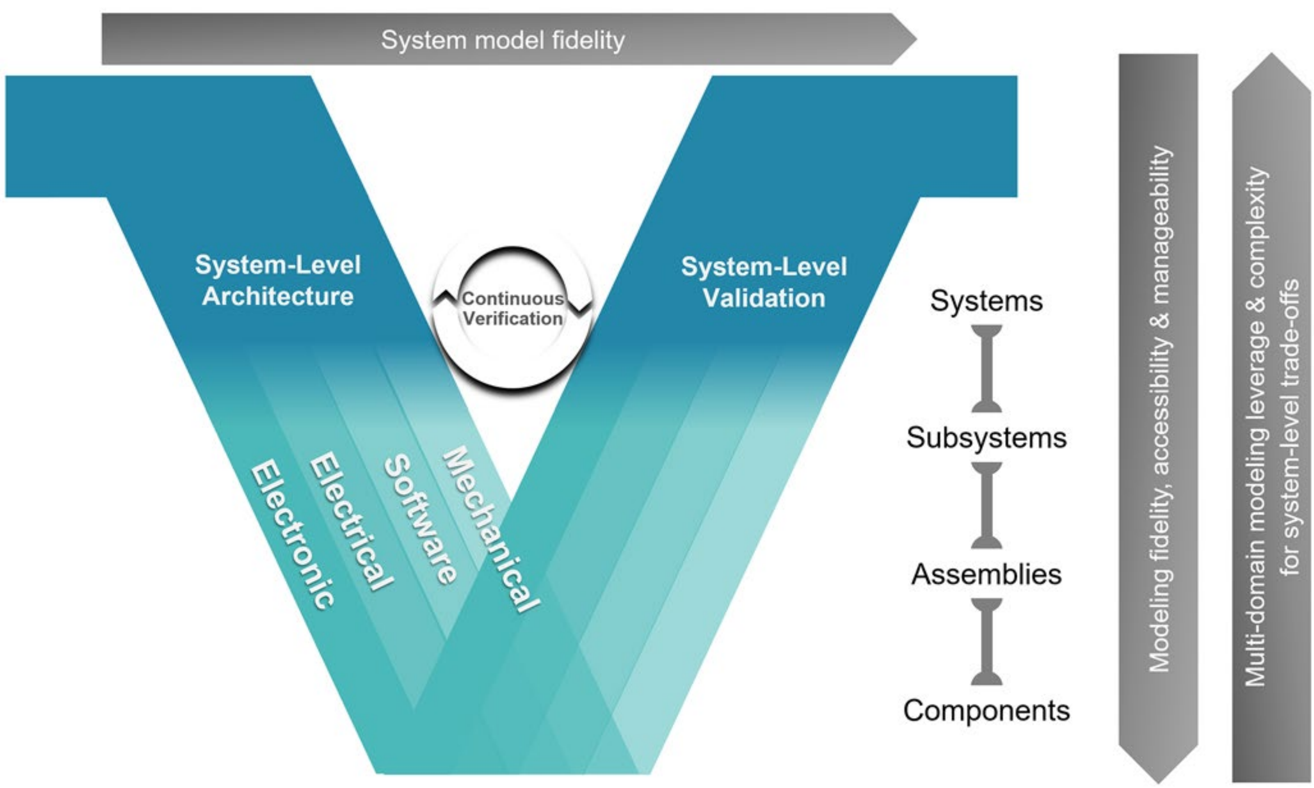


Figure1: Product development requires continuous verification throughout the design process, with a model of appropriate fidelity for each step.

of-systems. The goal is to go up the chain as far as possible.

The power of using digital twins across multiple domains could look like this example. You start with a board-level signal integrity simulation that gives some idea of the EMI radiating from that board. Then you use those results as part of modeling at the subsystem level, where you consider connectors and cablings and such things as the impact of a source harness against a victim harness, or the ability of the enclosure to contain radiation. Then you integrate more elements into that verified subsystem digital model to determine behaviors at the system level, where you're modeling things like the car, the antenna, and the placement of a motor in order to see how those things might impact 5G communication.

Only by integrating the domains together can we start to address system design challenges. Digital models, from components to systems, are required to connect the domains and enable early design optimization and verification, realizing the dream of a zero-spin design process. DESIGN007

David Wiens is Xpedition product manager for Siemens Digital Industries Software.
To read past columns or contact Wiens, click here.

BOOK EXCERPT

Introduction to *The Printed Circuit Designer's Guide to... High Performance Materials*

Choosing the right material for your application can be a major challenge. There are "cost to performance" decisions that need to be made in order to select material that will meet the expected performance requirements and the desired cost targets. Selecting a material that meets cost targets, but fails to perform in prototype development testing, results in costly revision spins, increases cost, and results in delays to market.

From the resin type, the styles and types of glass fabrics, and various types of copper foils, the reader can have a clearer picture of what to know when selecting which material is most desirable for their upcoming products. This book does not provide answers to all things laminate, but the hope is to provide a solid base for making material selection decisions and, along the way, answer some key questions like these:

- Why is PPO resin better than epoxy resin for electrical performance?
- Why could flat glass fabrics reduce the skew and ease for laser drilling?
- Why is very low-profile copper foil preferred for high-speed applications?
- What is the impact of raw material on data rate or on signal integrity testing?

When designs require high voltage CAF performance, thermal robustness, or high-speed massive data transmission rates, laminate materials must be selected to suit your requirements for printed circuit boards. The components used to make the laminates must be studied to know the influence on these kinds of applications.

This book was generated by key technical resources at Isola Group. Each of the contributing technical experts have 25–35 years of industry experience in laminate raw materials, laminate and prepreg manufacturing, laminate material development, new product introduction, PCB fabrication, and OEM applications. These individuals have contributed many years of tacit knowledge and experience, which are the basis for this book.

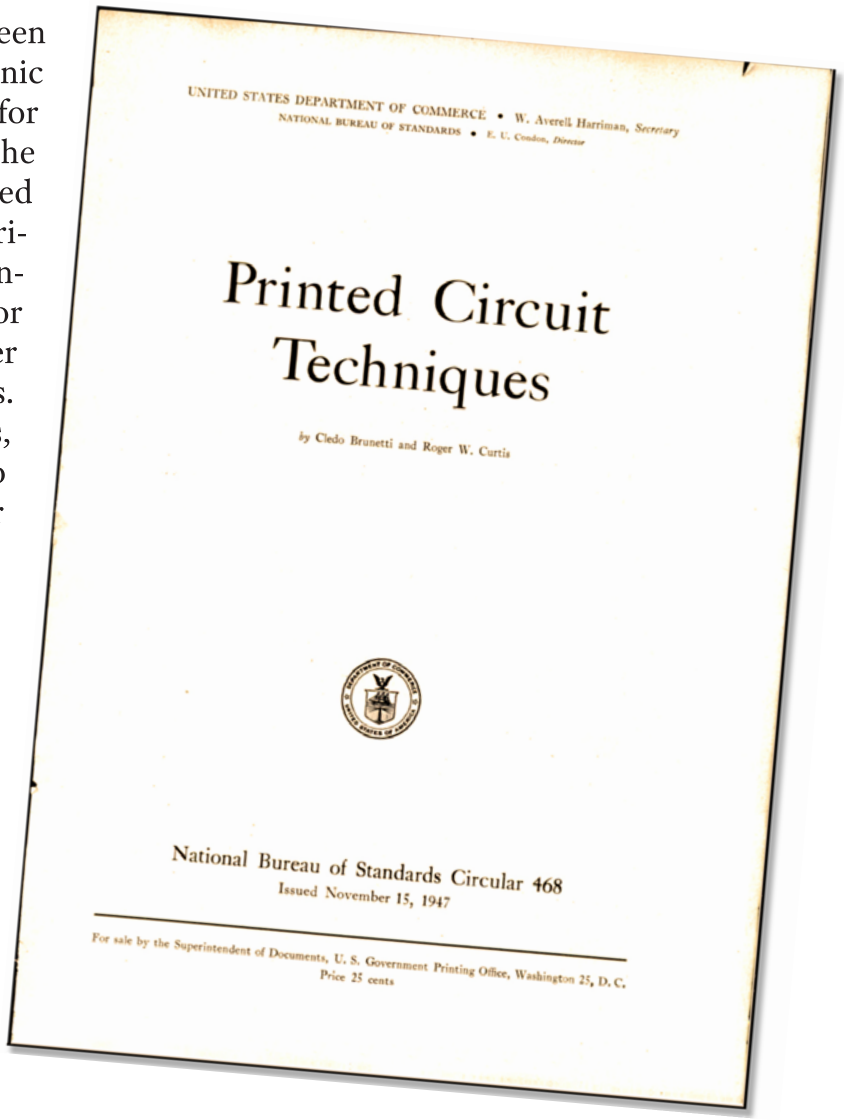
Download this book today!

Flexible Circuits or Flexible Electronics?

Flexible Thinking

by **Joe Fjelstad,** VERDANT ELECTRONICS

The term "flexible circuit" has been ensconced and accepted in electronic interconnection technology lexicon for several decades. In broad brush strokes the term has embraced every type of printed circuit produced on flexible base materials, regardless of the nature of the conductors used: metals, such as copper; or conductive inks, such as silver or other conductive particle filled polymers. The latter type of truly printed circuits, have, for many years, been referred to as "polymer thick film" circuits. Their predecessors were described in a Government Printing Office booklet published in 1947, titled "Printed Circuit Techniques." These circuits were easy and inexpensive to produce and were (and still are) commonly used to create membrane switch circuits for appliances and keyboards for every imaginable type of electronic product. Often, simple components were attached to these polymer and metal powder circuits using conductive adhesives to add


UNITED STATES DEPARTMENT OF COMMERCE • W. Averell Harriman, Secretary
NATIONAL BUREAU OF STANDARDS • E. U. Condon, Director

Printed Circuit Techniques

by Cledo Brunetti and Roger W. Curtis

National Bureau of Standards Circular 468
Issued November 15, 1947

For sale by the Superintendent of Documents, U. S. Government Printing Office, Washington 25, D. C.
Price 25 cents

function and versatility to the end-product while keeping costs low.

For many years, flexible circuits have also been designed to have components attached and integrated into what is called a flexible circuit assembly. In earlier years, flexible circuits played more limited roles as a means of providing a flexible link for conductors between rigid printed circuits or rigid PCBs and connectors. In the 1960s, the flexible circuit was integrated into a rigid printed circuit board by the visionary pioneering engineers at Sanders Associates in New Hampshire, yielding a product now commonly known and referred to as a rigid-flex circuit.

These terms were, and still are baseline, fundamental, widely understood, accepted by those in industry, and have been standardized. Standards were written to help codify issues related to flex circuit design, the materials used, as well as their manufacture, assembly, and performance. The IPC still leads that effort. As I have said in the past, I personally see standards as a sort of "industrial strength glue," if you will, that serves to hold the industry together and set expectations for product design, production, and performance.

Standards were written to help codify issues related to flex circuit design, the materials used, as well as their manufacture, assembly, and performance.

In 2015, NextFlex, an American consortium of electronics companies, academic institutions, and various nonprofits, along with several state, local, and federal government partners, was created. The group's self-reported charter was to promote what was historically known as printed flexible circuit technology. However, the founders decided, for reasons unknown, to form under a new name, "flexible electronics." It is arguable that such a new name was not really needed but it began the marketing of flex circuit technology under the new name, and in truth, it did help to bring flexible circuit technology into the sights of more people both in the industry and the general public.

The marketers did so with great determination, even to the point of changing the title of the content for flexible circuits found on Wikipedia from "flexible circuits" to "flexible electronics." That remains the case to this day—type the term "flexible circuits" into the search space on Wikipedia and view the results. As someone who deeply respects history and intellectual integrity, it seems an uncalled-for misappropriation of an accepted and decades long-established historical term and by doing so creating unnecessary confusion, as the product is still by original definition a flexible circuit. The term flexible electronics has since morphed to include "flexible hybrid electronics" (FHE) which involves the integration or assembly of active and passive devices.

To the credit of the newly formed community (which also includes SEMI's FlexTech), they have done good service to the electronic interconnection industry as evangelists for flexible circuits by attracting educators and academic technologists, encouraging them to envision and devise new ways to integrate flexible and stretchable circuits into next generation products of every imaginable type, especially wearable electronic devices. They have risen to the challenge as the variety of applications has continued to grow and, through the providing of a government sponsored environment, to explore those ideas. With the shared goal of advancing U.S. manufacturing of printed flexible electronics, the two entities have been promoting flexible circuit technology to the benefit of the entire flex circuit industry by raising awareness of the many benefits that flex circuits provide.

Since their launch under an Air Force Research Labs Cooperative Agreement, the NextFlex and FlexTech communities of technologists, educators, problem solvers, and manufacturers have come together to collectively facilitate the advancement of flexible interconnection technologies innovation by providing a space for shared research and material, process, and equipment development. It also serves as a training space for local students.

The long-established global and growing flexible circuit community will continue to thrive as increasing numbers of electronic product developers become aware of their potential to solve interconnection challenges. Flexible circuits, by any other name, will continue to be there to help make it happen just as the venerable technology has done since its inception many decades ago.

For those with interest in reading more on printing technologies for flex circuits, Chapter 11 in *Flexible Circuit Technology 4th Edition* (a free I-007eBook available for download) details the long history of the "new" technology of printed electronics. The chapter includes a review of traditional printing technologies such as screen printing, rotogravure printing, flexographic printing, and offset printing, as well as inkjet options. **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

LG Bolsters Leadership in 5G Vehicle Connectivity

LG's Vehicle component Solutions Company has proven that it has the technological knowhow and experience to lead the auto industry in the 5G era. According to market research firm Strategy Analytics, by 2026 approximately 67 million new vehicles worldwide will be equipped with telematics capabilities. Telematics 5G communications modules, introduced only last year, are expected to account for more than 25% of the total vehicle telematics market by 2026.

From vehicle-to-everything (V2X) systems to integrated hardware and software packages and in-vehicle communications gateways, LG's cutting-edge 5G telematics innovations deliver a new level of on-road connectivity and safety. An essential component in autonomous vehicles, V2X technologies enable vehicles to communicate in real-time with other vehicles, nearby pedestrians and infrastructure to create a safer environment for all.

Fast approaching the threshold for Society of Autonomous Engineers' Level 4 in which autonomous vehicles no longer require human interaction for operation, LG's 5G-V2X technology delivers more consistent vehicle data transmission speeds.

Utilizing Dual SIM Dual Active (DSDA) technology, LG's solutions simultaneously support connected car and autonomous driving functionalities, enabling vehicle occupants to enjoy entertainment services, convenient functions and enhanced safety. The 3rd Generation Partnership Project (3GPP) Release 16 5G module boasts significantly improved performance and more reliable connections. What's more, the smart, flat antenna allows automakers to maintain the aerodynamic lines of their designs which would be impossible with traditional "shark fin" antennas.

"Thanks to our experience and expertise in vehicle telematics, LG has been successful in winning a number of new contracts with established global automakers," said Eun Seok-hyun, president of the LG Vehicle component Solutions Company. (Source: PRNewswire)

Flex007 Highlights

ICAPE Group Acquires CEBISA France ▸

ICAPE Group and CEBISA France, a printed circuit board supplier based in Lisses (91), have signed an agreement to acquire 100% of CEBISA's activities by The French subsidiary of ICAPE Group. The transaction will be effective at the end of February.

Eltek Receives $1.4 Million Letter of Intent From Existing Defense Customer ▸

Eltek Ltd., a global manufacturer and supplier of technologically advanced solutions in the field of printed circuit boards, announced that the company has received a letter of intent for a purchase order in the amount of $1.4 million from an existing customer in the defense sector.

Real Time with... IPC APEX EXPO 2022: High-Tech Rigid-Flex Boards and More ▸

Jeff De Serrano, president of PCB Technologies for North America, and Editor Andy Shaughnessy discuss Jeff's current quest to acquire a PCB fabrication facility. Just six months into his new position at PCB Technologies, Jeff explains his plans for the next few years, including the company's focus on rigid-flex boards and their plans to invest heavily into high-tech substrates and microelectronics assembly.

Taiflex 2021 Revenue Up 7% YoY ▸

Taiwan-based Taiflex Scientific Co. Ltd, a manufacturer of flexible printed circuit materials such as flexible copper clad laminates (CCLs) and coverlays, has announced consolidated revenue of NT$801 million ($28.7 million at $1:27.87) in January 2022, up by 6.7% year-on-year (YoY), but almost flat from the previous month.

Rogers' Shareholders Approve Acquisition by DuPont ▸

Rogers Corporation announced that, at a special shareholder meeting, its shareholders voted to approve the previously announced acquisition of Rogers by DuPont de Nemours, Inc.

Real Time with... IPC APEX EXPO 2022: Rigid-Flex Specialists ▸

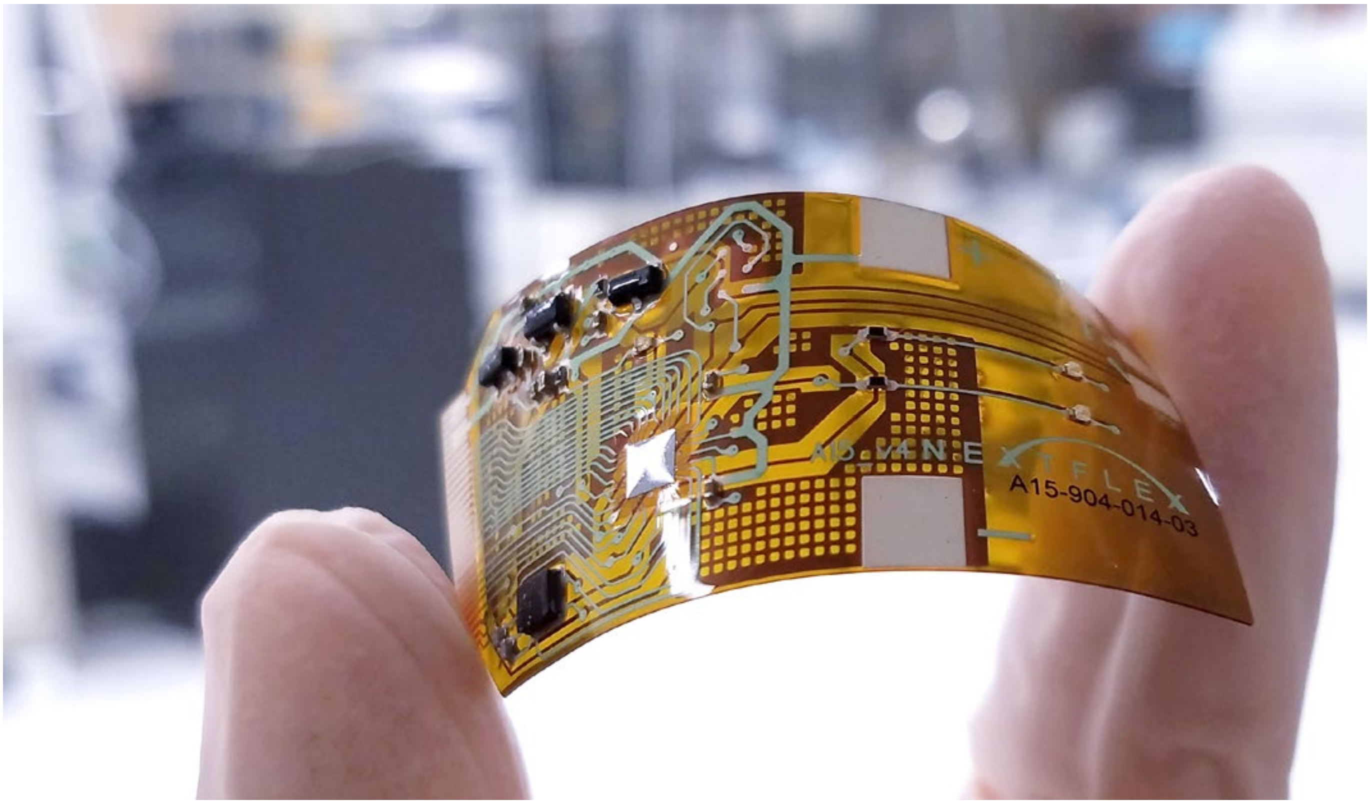
As flexible circuit specialists growing their worldwide business, Flexible Circuit Technologies is planning to expand its workforce. Chris Clark, senior applications engineer, discusses the company's 25% growth in the last year, as well as its new plant in Zhuhai, China, which will focus on rigid-flex circuitry. Chris just joined the company in the past year, but he has spent 31 years in the industry wearing whatever hat was required, and he lays out the company's plans for the next year.

Insulectro Printed Electronics Distributes Flexcon Products ▸

Insulectro, distributor of materials for use in manufacture of printed circuit boards and printed electronics, announced it will distribute FLEXcon® SWITCHmark® high-performance spacer components and laminating adhesives.

Compeq 2021 Sales Up 4% YoY ▸

Taiwan-based Compeq Manufacturing Co. Ltd has reported unaudited sales of NT$6.9 billion ($248.85 million at $1:NT$27.76) for December, up by 23.5% from December of last year, and by 1.2% from the previous month.



Flexible Hybrid Electronics Design: Reducing Time to Market

Article by Sean Nachnani
NEXTFLEX

Emerging innovations in the flexible hybrid electronics (FHE) domain are enabling new applications across multiple industries due to their highly flexible structures and additive manufacturing processes. The smaller form factor, lighter weight, and conformal capabilities are ideal for IoT edge devices in health and fitness monitoring, military asset identification and tracking, automotive displays and sensors, aerospace radar, and soft robotics. Significant industry research led by NextFlex is optimizing the processes from design through manufacture for FHE products.

FHE devices provide ideal solutions for many of today's conformal electronics needs. They allow for the implementation of SWaP-C (size, weight, power, and cost) improvements over their more traditional counterparts. Because these FHE devices bend and flex, however, the design process takes on more of an electromechanical approach. The final product application dictates certain features, such as static or dynamic bending, component placement, and material choices. Moreover, non-conventional flexible substrates and printed conductors require more extensive RF simulation and characterization, unique to each manufacturing process. Without proper tools or experience, these features can instead become detriments that lead to longer design cycles and increased costs. In this article, we will dive into the basics for FHE design and its requirements.

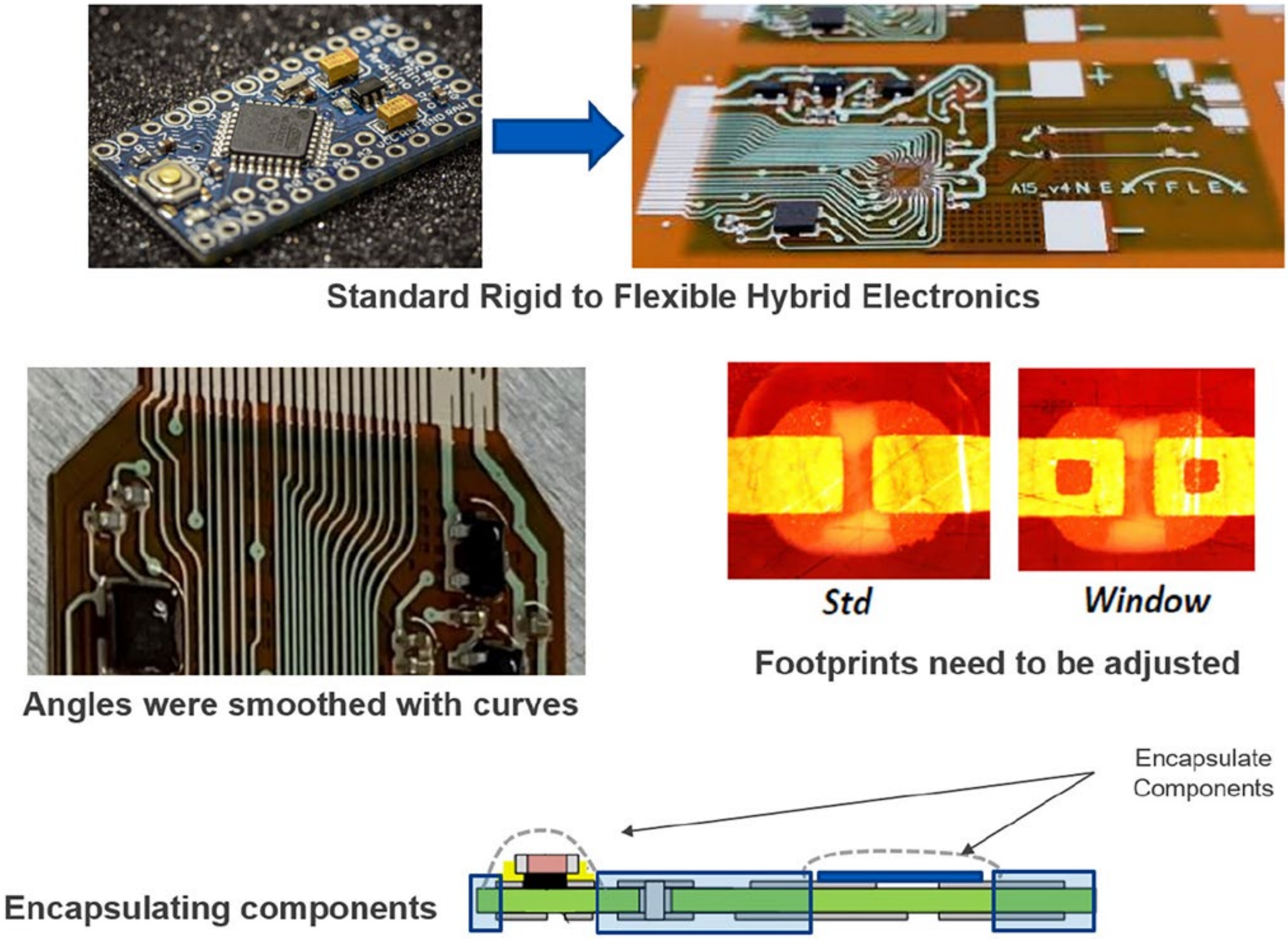


Figure 1: FHE design must account for differences between flexible and rigid PCBs.

We will discuss the tools NextFlex has developed to simplify the design process, shortening development cycles and ultimately time to market, and we will share how NextFlex and its consortium members from across the ecosystem are coming together to create materials databases and process development kits (PDK). We will describe how the materials and process database, FHE PDKs, reference designs, and managed reuse blocks are part of a new design process vision that promises to streamline FHE design and manufacturing.

Finally, we'll talk about how, through these efforts, new FHE reference designs are emerging, and how we'll be using these along with other reference modules to come up with a truly plug-and-play approach to FHE that reduces the amount of time and effort it takes to manufacture and design FHEs.

The Many Considerations When Designing for FHE

When it comes to designing FHE, its application drives the design considerations for the device as both a mechanical and electronic system. These considerations involve an interrelated set of choices based on application, environment, materials, process, and encapsulation.

FHEs have a wide variety of applications; for example, medical bandages that monitor vital statistics, monitoring systems for helicopter rotor blades, security tokens embedded into uniforms, and armbands that warn when a toxic gas concentration is too high. A primary question is whether the application will require a static bend form factor, where we apply the device and it stays as is, or will it be in dynamic, bending, and flex situations.

Then we need to look at the environment where these devices will be deployed. Are they being deployed in the middle of the desert, out on rough seas, in a cockpit above 30,000 feet, or is it on its way to the International Space Station?

Both target application and environment influence the material selection. What type of substrate and what type of inks will be used? Is this going to be a poly substrate or a polyethylene substrate? Will silver particle-free ink or nanoparticle ink be used? Perhaps not even silver at all; we may have to use copper carbon instead.

Material selection in turn drives process choices: how we actually manufacture the device and what type of process we use. Is it going to be a screen printer, an extrusion printer, an aerosol jet printer, or a combination of one of those along with a gravure offset printer or an ink jet printer. These all need to be considered before we even begin the process of designing the device.

Once we begin design work, we have to account for FHE being inherently different from the standard rigid PCB process. This truly is an electromechanical system, and we need to design for it as such. We need to design in how it will be bent or flexed, and we need to alleviate the mechanical stresses wherever possible to increase reliability and robustness. For example, we can apply curves instead of sharp angles, or we may apply teardrops onto the traces-to-pad junctions to help alleviate the stress in those areas as we bend the device.

We also need to investigate process dependent features. On a normal SMT for a rigid PCB, we might have just the standard 0402 or 0603 footprint. But for our additive process, if we're using silver ink, we might be using a conductive epoxy instead of a tin solder. So we need to design the pad footprints differently. They need to allow for adhesion to both the substrate and to the ink. We may need to add a non-conductive epoxy as well, to help secure the component to the device if it undergoes any mechanical stresses. Embedding components is an option as well with FHE. If we want to use printed passives, or if we have an ultra-thin die, we can embed them between layers.

Finally, encapsulation also affects how we apply and place components on the board. Are we going to use local encapsulation of the components or encapsulation of the entire device? Where do we place those components? Where do we group those components? Do we place mini-groups across the device to allow for both more rigid areas and more flexible areas? These are all questions that come with designing for FHE, and it's quite a few aspects to consider. How do we handle these multi-layered and interdependent considerations, choices, and processes in the most efficient and speedy manner possible?

Design Process Vision

We start with the materials and process database that feeds into the whole design process chain. Design process capabilities and constraints are fed from the materials and processes database into a FHE PDK, which is similar to an IC design PDK. The FHE PDK

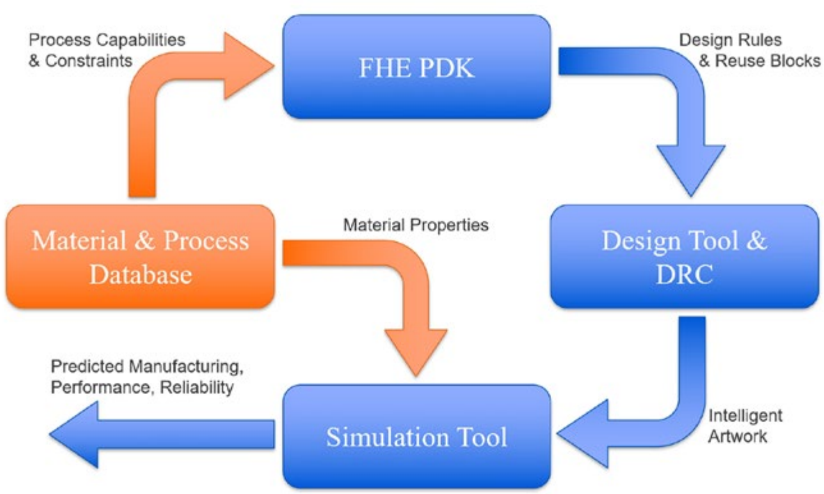


Figure 2: The FHE design process.

feeds into the design and layout tools, which help us with the FHE design and the design rule checks (DRC). The DRC feeds intelligent design artwork into the simulator, where we double-check our design against the specifications we've placed in it. The simulator also receives tested and validated properties from the materials and processes database. Ultimately, by following this design and process cycle, we come out with predictable manufacturing, predictable performance, and more reliable FHE devices.

Materials and Process Database

The materials and process database is the culmination of what we know about all the material interactions and the processes in place for FHE manufacturing. It contains the materials, substrates, inks, and encapsulants. It contains how they work together, how they don't work together, what their interactions are, how fine you can print on different processes, how large you can print conductivity, electrical properties, and materials.

The materials and process database is the culmination of what we know about all the material interactions and the processes in place for FHE manufacturing.

For example, we are running a three-phase study to produce a large amount of data that links process, materials, and performance for RF/antenna designs covering 0.4, 2.4, and 10 GHz. For this project we looked at fine-line test patterns and prints as well. The data collected covered a wide variety of materials, substrates, and ink combinations. We also took data from other projects that are focused on surface-mount and die attach. Through these, thousands of data records are being compiled into the NextFlex process and materials database, which we are generating for member access.

FHE Process Development Kit

Following the building of the materials and process database, the next step of the design process is the creation of the FHE PDK. A good way to think of the FHE PDK is as an interface that allows us to intelligently access data from the different databases and sources. The FHE PDK collects data from the materials and process database. Because these parts have been tested and validated, we can simply pull them into our design, knowing that there is simulated and tested data behind them.

The PDK also contains reliability test data: what the effects of thermal aging and humidity and bending are on our structures and systems. It includes the multi-physics models that are associated with that and the design rule checker. By associating a design rule checker with our PDK, when we create a design we can test it against different printing processes at different manufacturing sites.

This allows us a way to interface with the data from manufacturing sites, and it allows us to pick blocks and components that we know will work. Importantly, it allows us to start creating reuse blocks, or FHE IP blocks and modules. These modules enable us to start an FHE design, not from scratch, but by pulling known-good components and known-good blocks together to make our designs. This gives us all the advantages and benefits of a truly plug-and-play system, just like you would on an IC design PDK.

End users, IP developers, foundries, and everyone else in the ecosystem will benefit from this. Now we have a much easier way to develop FHEs. It's no longer tribal knowledge, but it's something that anyone can pick up using these tools. You don't have to spend the extra time going through costly redesigns and

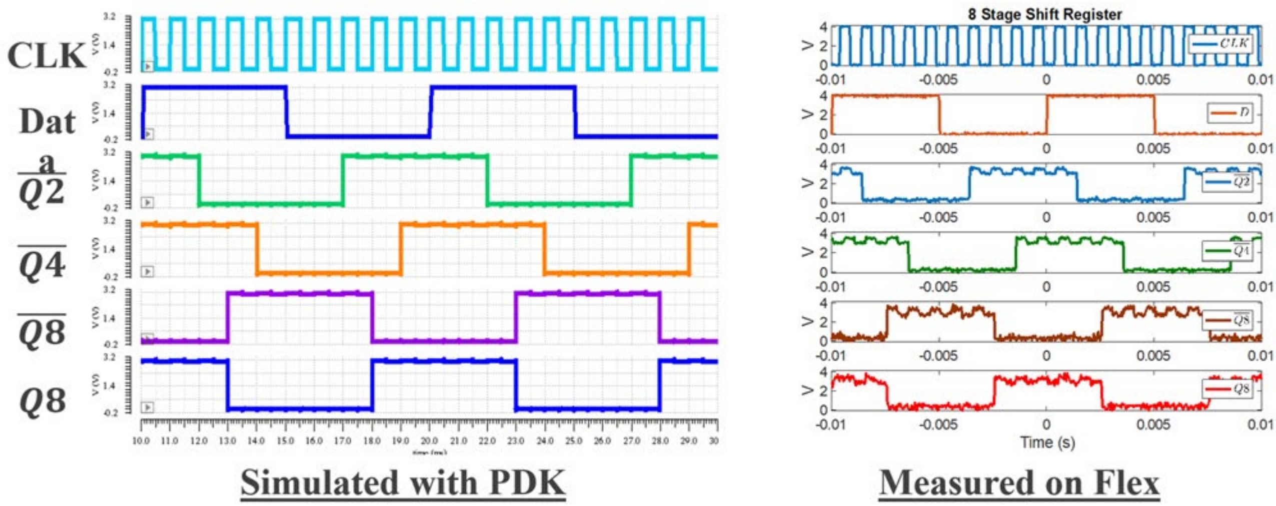


Figure 3: Expected and actual behavior of an FHE.

respins. You'll have validated, tested data that you know works, and validated designs that you know work. And the PDK interfaces well with the tools we use, such as the HyperLynx and Xpedition systems from Siemens EDA.

Now let's look at an example of an application of an FHE PDK for a flexible row driver that's turning on each call of the temperature sensor array, one by one, sequentially so that the readout circuitry and IO number can be shared and the pin count minimized. The graph on the left of Figure 3 was generated using the HyperLynx simulation tool. The design artwork and layout are ported into the tool, which simulates what the data is expected to be at different ports or different pins in the design. This allows us to accurately model and modify our designs to meet the requirements we want. This represents the intended, ideal model of the system and how it should act.

The graph on the right shows the measured data of that same system. It reveals that the intended behavior is represented very accurately. It's so accurate because we're using the FHE PDK. In other words, we're using validated, tested models when we're running the simulation. If we didn't have the PDK, then we could still achieve these results, but it would require a lot more cycle time. We'd have to go through multiple redesigns and potentially feed all that measured data into the simulation to refine it to get to this level of results. With the FHE PDK, all you do is pull out the known components, the known modules, into your design, simulate it, and you know you're going to get a manufacturing result that matches your simulation.

FHE PDK DRC

Now let's examine how we use the PDK for design rule checking (DRC). For DRC, we can import a design. Let's say we just finished a new layout for a new FHE design. It's a great device, with a lot of different sensors and LEDs, and we want to see if we can manufacture it. Let's say we want to manufacture it at the NextFlex facility using a screen print. We'd load up the DRC, load in the rule check for screen print, and we'd run it, and the DRC would do all the hard work.

It will generate the violation report if there's any violations. It will tell us if the vias are too close, if it's below the minimum spacing allowed, or if a trace is too thin or too thick. And it makes it easy to see what design changes are needed, if any, to run it through a specific manufacturing process. It can be run for any of the printing processes: screen print, inkjet, extruded, etc.

Overall, we see that the PDK plays an instrumental role in reducing the amount of time and

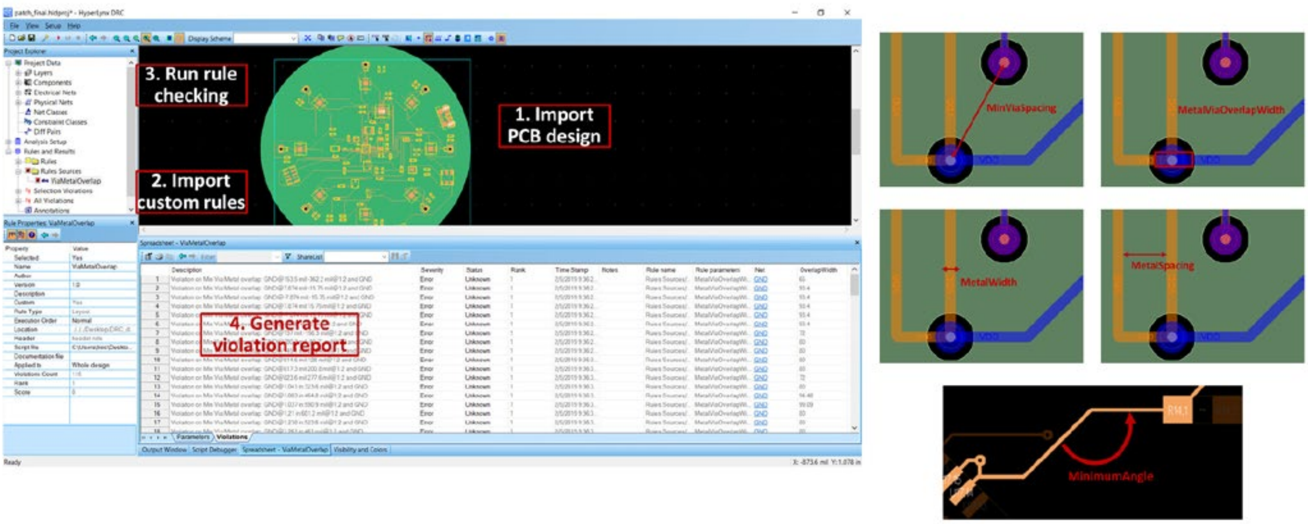


Figure 4: Using HyperLynx DRC on an FHE PDK.

effort it takes to design and manufacture FHE devices.

Reference Designs and Managed Reuse Blocks

Now that we've seen how the materials database and the FHE PDK streamline the FHE design and manufacturing aspects, we will move on to what is one of the more important steps in the FHE design process: reference designs and managed reuse blocks.

With these reference designs, when you start a brand new FHE design, you don't have to design and pull together everything from scratch. Because you don't have to create it from scratch, you don't have to go through all the effort of creating both the physical and the logical design for whichever manufacturing process you're using. You just pick it from the managed library, and you add the connections between the blocks, and that's it. That's the plug-and-play approach that we're developing to really accelerate product development in the FHE space.

For example, if you want Bluetooth, you simply pull the module that supports Bluetooth 5. If you want wireless charging, you pull the wireless charging module. If you want environmental sensing, you pull the modules that provide those aspects. Obviously, this simplifies the entire process and greatly simplifies the designing aspect.

To show how we're using that capability in our actual designs, let's look at our first reference design. This is based off the semiconductor nRF52840 Bluetooth 5 IC. This device uses an ultra-thin 50-micron thick, thinned bare die,

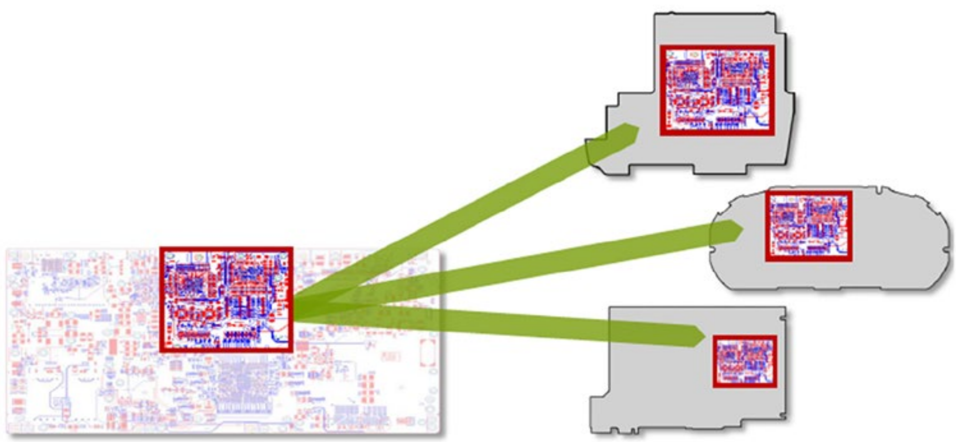


Figure 5: Reuse of known-good circuit blocks accelerates the design process.

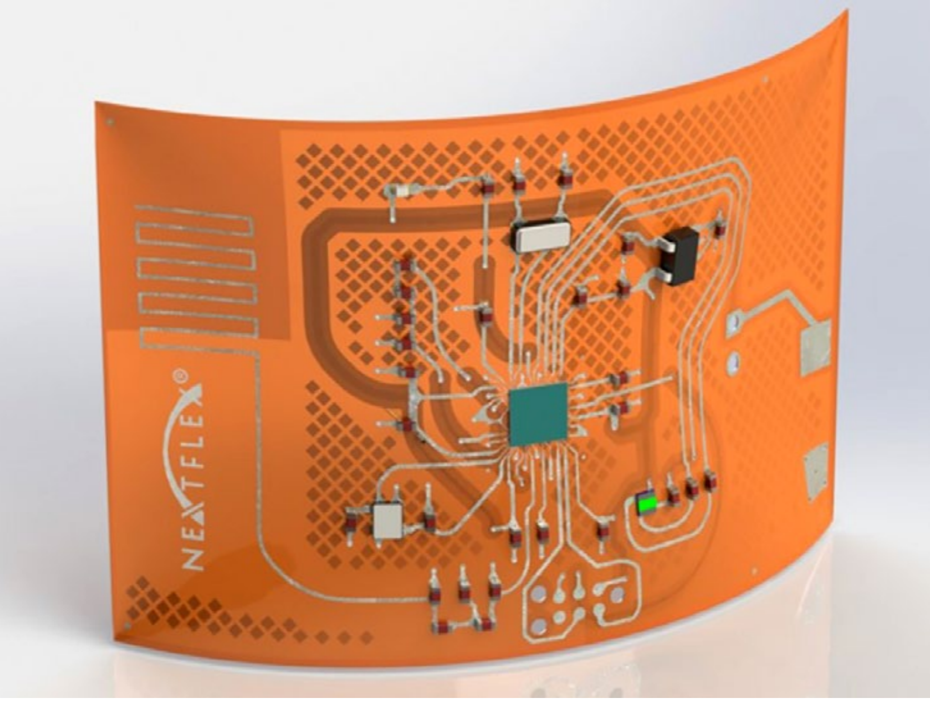


Figure 6: Nordic Semiconductor nRF52840.

and its flip-chip attached to the traces. This reference design uses screen printing, and it also uses a laser ablation approach to get to the fine feature sizes needed for a flip-chip attach. It also includes an external battery connection and a printed Bluetooth 5 antenna. The reference design contains the core Nordic Semi components that enable the chip to broadcast over Bluetooth as well as an RGB LED. By starting with this reference design, you can just attach any additional sensors and any additional components that you bond to create your Bluetooth module in FHE design.

The second reference design focuses on a different family of microcontrollers, namely the RSL10 series from ONSemiconductor. This design contains a system in package (SiP) instead of a bare die. This SiP also has a Bluetooth 5 antenna integrated with the RSL10 microcontroller. Because of the package type, it also allows for printing with a wider variety of processes as it's not as fine pitched as the Nordic Semiconductor bare die flip-chip. It also contains a couple of unique features: onboard circuitry that allows it to be fully operational with an external solar cell, either outdoors or indoors, and the ability to pull data from its BME280 or BME456 onboard sensors.

Both reference designs are starting points. They will enable the first iterations of new FHE devices for our community members. And going forward we plan to add in more and more of these modules to our library database, to this ecosystem. So ultimately, what we'll end up with is an entire library of modules that allows us to truly plug-and-play. When we're coming to a new design, we just pick the modules and that's it, it'll significantly reduce the time it takes to bring a device to the manufacturing step.

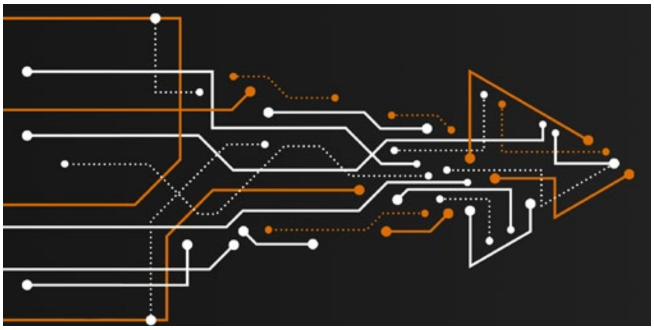
I'd like to finish with a few points. First, FHE requires new design and simulation approaches. It's inherently different from traditional electronics manufacturing, and new processes are required.

Second, a broad engagement is needed from the manufacturing ecosystem. We're dealing with new processes and novel manufacturing. Only engagement from everyone in the ecosystem—the chip makers, end users, materials manufacturing, and all those in between—will propel this effort forward. Finally, with all the work that's been ongoing with the materials databases and the PDKs, we're finally able to provide plug-and-play designs built to provide modules that not only enable a faster turnaround but also reduce the amount of time and effort it takes to manufacture and design for FHE. **FLEX007**

Sean Nachnani is a hardware systems engineer with NextFlex. This article originally appeared as a white paper published by Siemens Digital Industries Software.

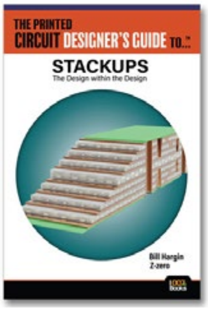
TOP TEN
EDITOR'S PICKS

PCB Talk: SAP Evaluating From Design Perspective



Semi-Additive PCB fabrication processes add a new tool to the PCB designer's toolbox. As with any new tool, there is a learning curve. To help shorten that curve and expand the growing body of knowledge, Tara Dunn speaks with Randy Chase, CID. He is the senior manager of PCB and Module Design at pSemi, a Murata company.

Finally! A Book About PCB Stackups



The Printed Circuit Designer's Guide to... Stackups: The Design within the Design is the latest addition to I-Connect007's library. In this book, brought to readers by Siemens Digital Industries Software and I-007eBooks, author and stackups expert Bill Hargin discusses materials, laminate datasheets, impedance planning, and more, providing the reader with a broader understanding of stackup planning and material selection.

High-Voltage Circuit Design Guidelines and Materials

The Hubble telescope, the Cassini-Huygens mission, and other exploratory spacecraft utilize high-voltage DC power supplies for everything from vidicon camera tubes and mass spectrometers to radar and laser technologies. NASA has experienced performance problems with the 1.5 kV supplies because—as a 2006 report stated—"designers did not take the high-voltage problems seriously in the initial design."

AltiumLive 2022: Keep Your Boards From Screaming with Eric Bogatin's EMI Tips


Eric Bogatin

Signal integrity evangelist Eric Bogatin talks about his AltiumLive keynote presentation, "How to Keep Your Boards from Screaming Like a Banshee." Eric explains how attention to board structures during the early stages of PCB layout can keep EMI from becoming a problem in your design.

Real Time with... IPC APEX EXPO 2022: Selecting the Right Base Material

Editor Andy Shaughnessy sat down with Steven Sekanina, Isola's director of High Speed Digital Products, to discuss the importance of selecting the right base material for your printed circuit board, and the criteria to consider when choosing high-speed PCB laminates.

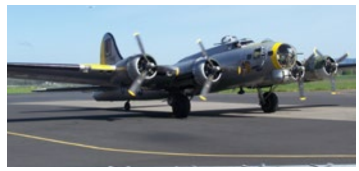
Sensible Design: Top Design Tips for a Successful Coating Process

This month's column highlights some of the key challenges and commonly asked questions about conformal coatings that every design engineer should take into consideration when specifying the coating process.

AltiumLive 2022: Don't Phone It In—Reducing EMI in Wireless Applications

I recently spoke with Ken Wyatt, founder of Wyatt Technical Services and an expert on signal integrity and EMC. I asked him to discuss his AltiumLive 2022 presentation, which focuses on reducing EMI, particularly in the wireless arena, where self-generated emissions are often a fact of life.

Tim's Takeaways: The Misadventures of High Voltage and Other Related Problems with Power



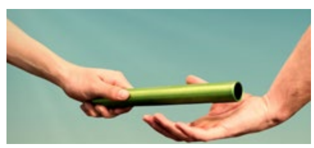
If you've read my column before you know how much of a fan I am of aviation, especially when it comes to older airplanes. You can imagine how ecstatic I was when, 11 years ago, my wife gave me the greatest gift of all; a half-hour ride on a fully restored WWII B-17 Flying Fortress.

Kris Moyer Discusses New IPC Design Role

Kris Moyer

The I-Connect007 editorial team spoke with Kris Moyer, a longtime PCB designer who has just joined IPC's Education Foundation. Kris was one of the judges and creators of the IPC Design competition that culminated at IPC APEX EXPO, and he was eager to discuss his new job and the cutting-edge technology he's seen lately, including additive, flex, and rigid-flex circuits.

Digital Transformation: Seamless Hand-off from Design to Manufacturing



Without a seam. That's what seamless means. There is no evidence of the transition from one material to another, or in the case of processes, from one process to another. That is the goal of everyone in the PCB ecosystem—designers, fabricators, and contract manufacturers alike.

For the latest news and information, visit **PCBDesign007.com**

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In addition, your ad will:

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Potential candidates can click on your ad and submit a resume directly to the email address you provide, or be directed to the URL of your choice.

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R&D Scientist III, Orange, CT

Job Description: The scientist will be a leader in technology for plating chemistry development, electrolytes, and additives. The position is hands-on, where the ideal candidate will enjoy creating and testing new aqueous plating processes and materials to meet the most demanding semiconductor applications related to Wafer-Level Packaging and Damascene. The qualified candidate will work as part of the R&D team while interacting with scientists, product management, and application engineers to commercialize new products for the advanced electronic solution business.

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Prototype Engineer, Sawanee, GA

Job Description: The purpose of this position is to provide direct technical and customer support for the Electronic Polymers (EP) product line of the Semiconductor Solutions Group for existing products as well as new and developmental products. The position is responsible for leading the team with customer builds and proof of concept designs directly engaging with customers. The position will lead a variety of technical, customer support, quality, marketing, process, and production related projects.

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Regional Manager

Midwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the States of IL, IN & MI. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
  - Reviews progress of sales performance
  - Provides quarterly results assessments of sales reps' performance
  - Works with sales reps to identify and contact decision-makers
  - Setting growth targets for sales reps
  - Educates sales reps by conducting programs/seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

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Career Opportunities

INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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ventec INTERNATIONAL GROUP 騰輝電子

Customer Service Representative

Fullerton (CA) USA

(and) **Elk Grove Village (IL) USA**

Ventec is looking to expand our Customer Service/Internal Sales team at our facility in Fullerton, California, and Elk Grove Village, Illinois.. As Customer Service Representative you will provide great sales and customer service support and respond to the needs of clients from industries including Aerospace, Defense, Automotive and Pharmaceutical. Duties include:

- Maintain and develop both existing and new customers through individual account support
- Make rapid accurate cost calculations and provide customers with quotations
- Accurately input customer orders through the company's bespoke MRP System
- Assist the sales team with reporting, sales analysis, and other items at their request
- Liaise with colleagues at Asia HQ and Overseas Business Units to manage domestic and international requirements

Required Skills and Abilities

The ideal candidate is a proactive self-starter with a strong customer service background. Friendly, approachable, and confident, you should have a good phone mannerism and be computer literate.

- Previous experience in a Customer Service background, ideally management or supervisor role
- Experience with MRP Systems
- Good working knowledge of Microsoft Office Tools such as Outlook, Excel etc

What's on Offer

- Excellent salary & benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

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MacDermid Alpha
ELECTRONICS SOLUTIONS

Engineering Project Manager Graphics/Film

The primary purpose of this position is to manage Process Development, Process Scale Up and Capital projects in the Global Process Engineering Group (GPEG) function.

THIS INCLUDES:

- Managing the complete life cycle of the highly complex projects including approval of the projects, the planning and execution of the projects, and then the closeout of the projects to ensure planned results are achieved on a timely basis.
- Develop budgets timelines, and ensure progress to plan, as well as tracking project achievements.
- Define projects' objectives and ensure progress to plan, as well as tracking project achievements.
- Interface with internal customers to agree upon specifications, deliverables, and milestones.
- Represent project and the team and present project results to customers and internal management.
- Recommend new process and tools to achieve advanced project management.
- Manage project status in the form of formal briefings, project update meetings, and written, electronic, and graphic reports.
- Address problems through risk management and contingency planning and present solutions and/or options to executive management.

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ELECTRONICS SOLUTIONS

Technical Marketing Specialist

Waterbury, CT

JOB DESCRIPTION:
Responsible for providing technical knowledge and support to marketing communications professionals. Cross training and acting as liaison between the Innovation and the Marketing Communications teams for both Circuitry Solutions and Semiconductor Solutions.

Chemist 1

Waterbury, CT

JOB DESCRIPTION:
Perform analysis—both chemical and mechanical—of customer-supplied samples. These include both structural and chemical testing using various instruments such as SEM, Instron, ICP, and titration methods. Perform various failure analysis functions, including, but not limited to, chemical analysis, SEM analysis of customer parts, and cross-section evaluation.

Applications Manager

Waterbury, CT/New England Region

JOB DESCRIPTION:
Applications Manager in the Electronics Specialties/Circuitry Solutions group to provide applications process knowledge, training and technical support of new products leading to sales revenue growth. Requires working through the existing sales and technical service organizations to leverage this knowledge globally. Experience in multilayer bonding along with dry film and solder mask adhesion processes a plus.

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Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

Wet Process Engineer

ASC, the largest independent PCB manufacturer in the Midwest, is looking to expand our manufacturing controls and capabilities within our Process Engineering department. The person selected will be responsible for the process design, setup, operating parameters, and maintenance of three key areas—imaging, plating, etching--within the facility. This is an engineering function. No management of personnel required.

Essential Responsibilities

Qualified candidates must be able to organize their own functions to match the goals of the company.

Responsible for:

- panel preparation, dry film lamination, exposure, development and the processes, equipment setup and maintenance programs
- automated (PAL line) electrolytic copper plating process and the equipment setup and maintenance programs
- both the cupric (acid) etching and the ammoniacal (alkaline) etching processes and the equipment setups and maintenance programs

Ability to:

- perform basic lab analysis and trouble-shooting as required
- use measurement and analytical equipment as necessary
- work alongside managers, department supervisors and operators to cooperatively resolve issues
- effectively problem-solve
- manage multiple projects concurrently
- read and speak English
- communicate effectively/interface at every level of the organization

Organizational Relationships

Reports to the Technical Director.

Qualifications

Degree in Engineering (BChE or I.E. preferred). Equivalent work experience considered. High school diploma required. Literate and functional with most common business software systems MS Office, Excel, Word, PowerPoint are required. Microsoft Access and basics of statistics and SPC a plus.

Physical Demands

Exertion of up to 50 lbs. of force occasionally may be required. Good manual dexterity for the use of common office equipment and hand tools.

- Ability to stand for long periods.

Work Environment

This position is in a manufacturing setting with exposure to noise, dirt, and chemicals.

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MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and x-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

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Ucamco

Sales Engineer

Germany, Austria, Switzerland, Southeastern Europe e.g. Italy

Ucamco is looking for a sales engineer for our front-end software in the German-speaking area (Germany, Austria, German Switzerland) as well as adjacent markets in the South and East.

Ucamco is a market leader in PCB CAM, pre-CAM software and laser photoplotters with more than 35 years' experience developing and supporting leading-edge, front-end tooling solutions for the global PCB industry.

Responsibilities:

- Selling software solutions
- Selling support contracts and upgrades
- Developing and implementing customer acquisition plan
- Organizing and taking part in roadshows, seminars, exhibitions
- Follow up of current customers and sales
- Contributing insights into the marketing plan
- Reporting to Ucamco's sales director

Requirements:

- Fluent in German, good knowledge of English; other languages a plus
- Frequent traveling to prospects and customers–live contact is important
- Feeling for technical software
- Motivated to succeed as a solution seller
- Strong empathy for the customer
- Self-starter, able to work independently, organized
- Honest, trustworthy, dependable, credible
- Sales and technical expertise in PCB industry a big plus
- Knowledge of market and customer base in German speaking area a big plus
- Used to working from home office
- Traveling to headquarters in Gent (Belgium) for sales and customer meetings
- Good feeling for software is more important than strong sales experience

This is a salary-based position with a commission plan, company car, expense reimbursement, and benefits like health insurance.

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Printed Circuits, a fast-growing printed circuit board fabricator, offers:

- Excellent opportunities for advancement and growth
- Dynamic manufacturing environment
- Excellent health, dental and other benefits
- Annual profit-sharing plan
- Signing bonus
- Additional incentives at the leadership level
- Clean facility with state-of-the-art manufacturing equipment
- Highly collaborative corporate and manufacturing culture that values employee contributions

Laminator Technician

Nature of Duties/Responsibilities

- Layup cover lay
- Layup rigid flex
- Layup multilayer/CU core boards
- Oxide treat/cobra treatment of all layers/CU cores
- Shear flex layer edges
- Rout of machine panel edges and buff
- Remove oxide/cobra treatment (strip panels)
- Serialize panels
- Pre-tac Kapton windows on flex layers (bikini process)
- Layup Kapton bonds
- Prep materials: B-stage, Kapton, release sheet
- Breakdown: flex layers, and caps
- Power scrub: boards, layers, and caps
- Laminate insulators, stiffeners, and heatsinks
- Plasma cleans and dry flex layers B-stage (Dry)
- Booking layers and materials, ready for lamination process
- Other duties as deemed necessary by supervisor

Education/Experience

- High school diploma or GED
- Must be a team player
- Must demonstrate the ability to read and write English and complete simple mathematical equations
- Must be able to follow strict policy and OSHA guidelines
- Must be able to lift 50 lbs
- Must have attention to detail

Wet Process/Plating Technician

Position is 3rd shift (11:00PM to 7:30AM, Sunday through Friday)

Purpose

To carry out departmental activities which result in producing quality product that conforms to customer requirements. To operate and maintain a safe working environment.

Nature of Duties/Responsibilities

- Load and unload electroplating equipment
- Fasten circuit boards to racks and cathode bars
- Immerse work pieces in series of cleaning, plating and rinsing tanks, following timed cycles manually or using hoists
- Carry work pieces between departments through electroplating processes
- Set temperature and maintains proper liquid levels in the plating tanks
- Remove work pieces from racks, and examine work pieces for plating defects, such as nodules, thin plating or burned plating
- Place work pieces on racks to be moved to next operation
- Check completed boards
- Drain solutions from and clean and refill tanks; fill anode baskets as needed
- Remove buildup of plating metal from racks using chemical bath

Education and Experience

- High school diploma or GED required
- Good organizational skills and the ability to follow instructions
- Ability to maintain a regular and reliable attendance record
- Must be able to work independently and learn quickly
- Organized, self-motivated, and action-oriented, with the ability to adapt quickly to new challenges/opportunities
- Prior plating experience a plus

Production Scheduler

Main Responsibilities

- Development and deployment of a level-loaded production plan
- Establish manufacturing plan which results in “best possible” use of resources to maximize asset utilization
- Analyze production capacity of manufacturing processes, equipment and human resource requirements needed to produce required products
- Plan operation manufacturing sequences in weekly time segments utilizing production labor standards
- Maintain, align, and communicate regularly with internal suppliers/customers and customer service on key order metrics as per their requirements
- Frequently compare current and anticipated orders with available inventory and creates replenishment plan
- Maintain master distribution schedule for the assigned facility, revise as needed and alert appropriate staff of schedule changes or delays
- Participate in periodic forecasting meetings
- Lead or participate in planning and status meetings with production, shipping, purchasing, customer service and/or other related departments
- Follow all good manufacturing practices (GMPs)
- Answer company communications, fax, copy and file paperwork

Education and Experience

- High school diploma or GED
- Experience in manufacturing preferred/3 years in scheduling
- Resourceful and good problem-solving skills
- Ability to make high pressure decisions
- Excellent written and verbal communication skills
- Strong computer skills including ERP, Excel, Word, MS Office
- Detailed and meticulous with good organizational skills
- Must be articulate, tactful and professional at all times
- Self-motivated

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Career Opportunities

Manncorp™

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

apply now

Manncorp™

SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

apply now

Career Opportunities

OMRON

SPI AOI AXI

Account Manager (SPI | AOI | AXI)

Omron Automation Americas is actively seeking an energetic and focused Account Manager to help support our Automated Inspection Solutions product business (SPI, AOI and AXI).

This position is based within any major city covering the Western-US region (including Dallas, Austin, Phoenix and Northern/Southern California). The goal is to work independently and alongside our strong rep. partners in the territory to further expand our business in industries and market segments where we have high potential for continued success and growth.

This is a rare opportunity to join the dynamic team of professionals at Omron and work for a true, industry leader.

To learn more about this exciting role, please contact us directly via:

shawn.arbid@omron.com

apply now

Prototron Circuits

Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB shop, is looking for sales representatives for all territories.

Reasons you should work with Prototron:

- Serving the PCB industry for over 30 years
- Solid reputation for on-time delivery (99% on-time)
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- AS9100
- MIL-PRF- 31032
- ITAR
- Global sourcing
- Engineering consultation
- Completely customer focused team

Interested? Let's have a talk.
Call Dan Beaulieu at
207-649-0879
or email to
danbbeaulieu@aol.com

apply now

Career Opportunities

The Test Connection, Inc.

Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/ Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

apply now

Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

apply now

Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/ GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

Contact us today to learn about the rewarding careers we are offering. Please email resumes with a short message describing your relevant experience and any questions to careers@ttci.com. Please, no phone calls.

We proudly serve customers nationwide and around the world.

TTCI is an ITAR registered and JCP DD2345 certified company that is NIST 800-171 compliant.

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Career Opportunities

Career Opportunities

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

apply now

SIEMENS

Siemens EDA Sr. Applications Engineer

Support consultative sales efforts at world's leading semiconductor and electronic equipment manufacturers. You will be responsible for securing EM Analysis & Simulation technical wins with the industry-leading HyperLynx Analysis product family as part of the Xpedition Enterprise design flow.

Will deliver technical presentations, conduct product demonstrations and benchmarks, and participate in the development of account sales strategies leading to market share gains.

- PCB design competency required
- BEE, MSEE preferred
- Prior experience with Signal Integrity, Power Integrity, EM & SPICE circuit analysis tools
- Experience with HyperLynx, Ansys, Keysight and/or Sigrity
- A minimum of 5 years' hands-on experience with EM Analysis & Simulation, printed circuit board design, engineering technology or similar field
- Moderate domestic travel required
- Possess passion to learn and perform at the cutting edge of technology
- Desire to broaden exposure to the business aspects of the technical design world
- Possess a demonstrated ability to build strong rapport and credibility with customer organizations while maintaining an internal network of contacts
- Enjoy contributing to the success of a phenomenal team

***Qualified applicants will not require employer-sponsored work authorization now or in the future for employment in the United States. Qualified Applicants must be legally authorized for employment in the United States.*

apply now

Career Opportunities

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- Engineering
- Quality
- Various Manufacturing

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

Career Opportunities

U.S. CIRCUIT

Plating Supervisor

Escondido, California-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package.
Pay will be commensurate
with experience.

Mail to:
mfariba@uscircuit.com

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YOUR JOB AD HERE

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