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JUNE 2021

DESIGN007 MAGAZINE

SPACE AND TRACE: THE FINAL FRONTIER

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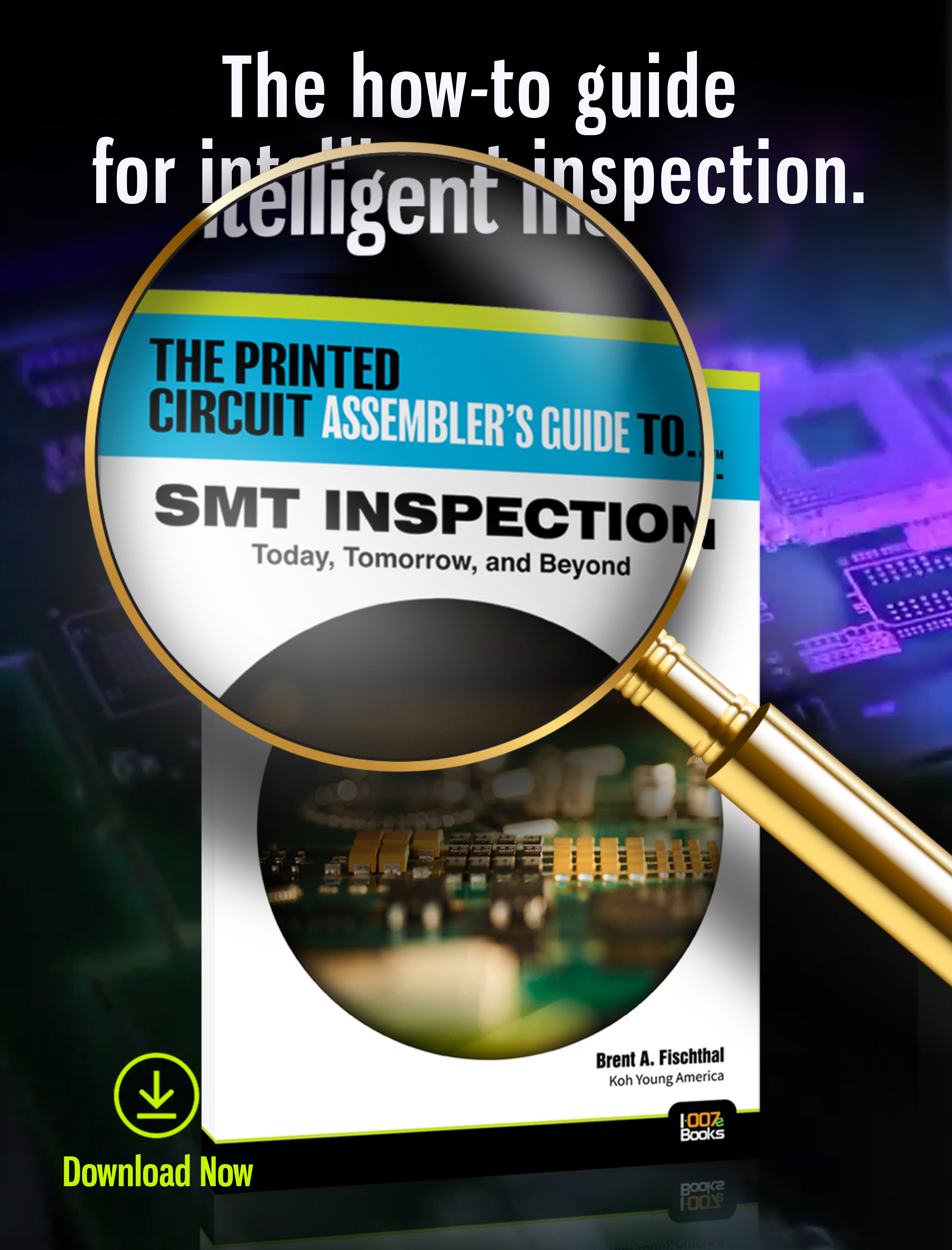
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SPACE AND TRACE, THE FINAL FRONTIER

This month, we're helping William Shatner celebrate his 90th birthday with an issue devoted to *Star Trek*. Our intrepid Trekkie contributors delve into some of the technological marvels introduced on the show, and they take a look back at how far PCB design and manufacturing technology has come since that first episode, "The Man Trap," debuted in 1966, winning its time slot in the Nielsen ratings.

FEATURES

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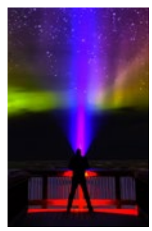
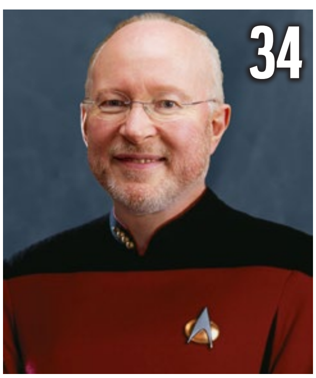
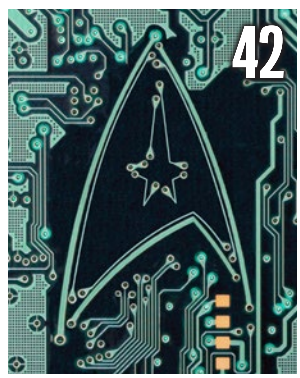
FEATURE COLUMNS







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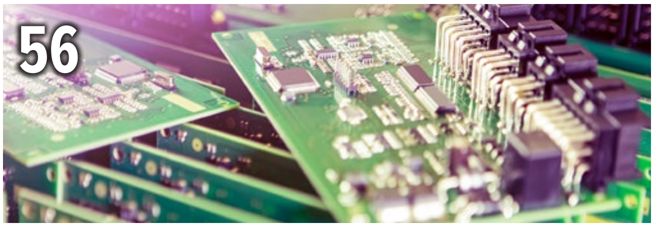

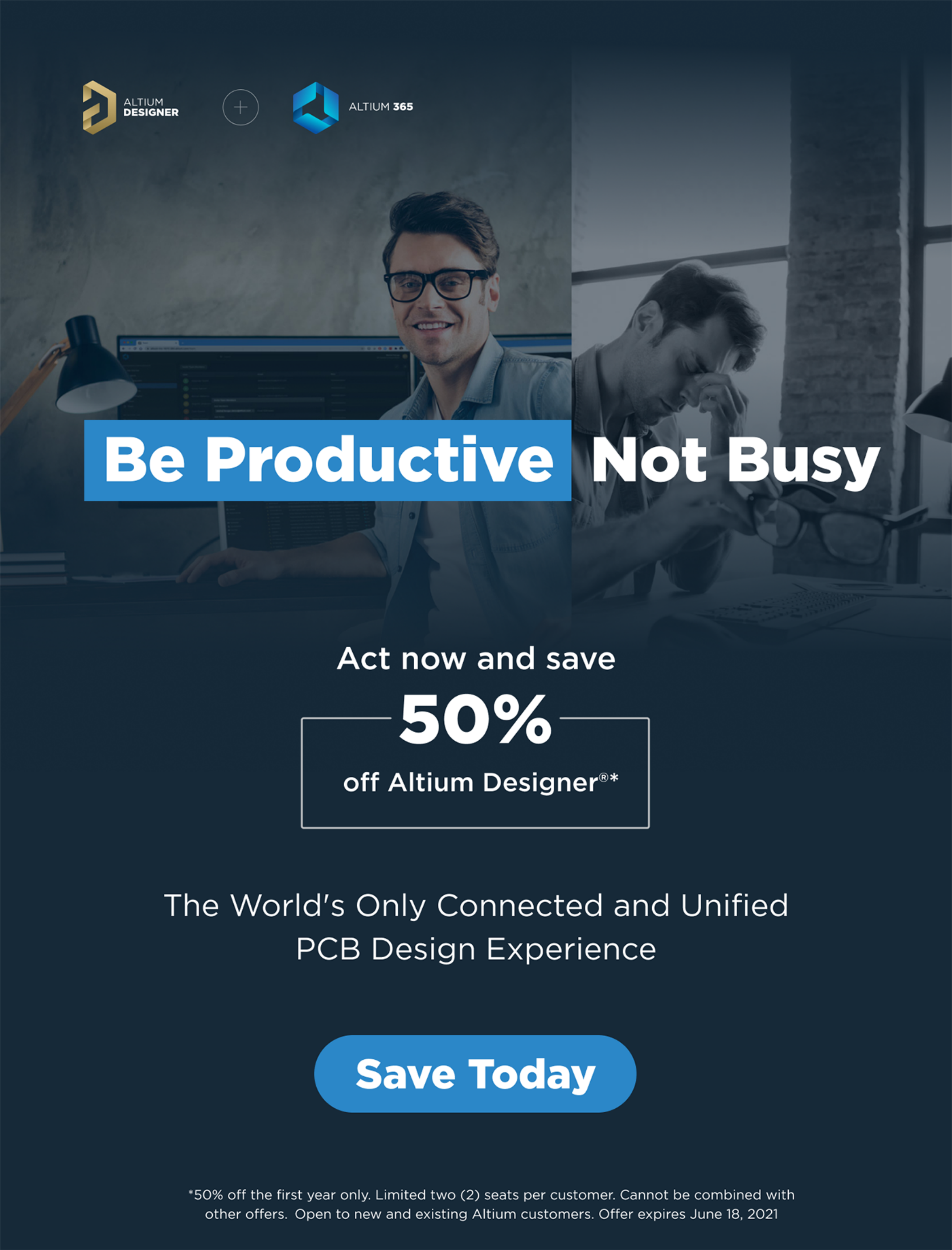
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FLEX007

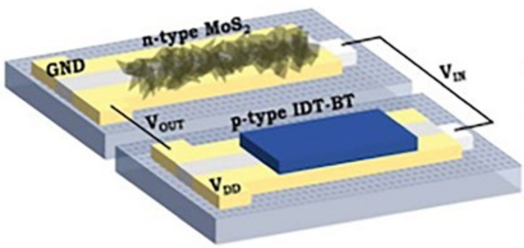
This Month in Flex

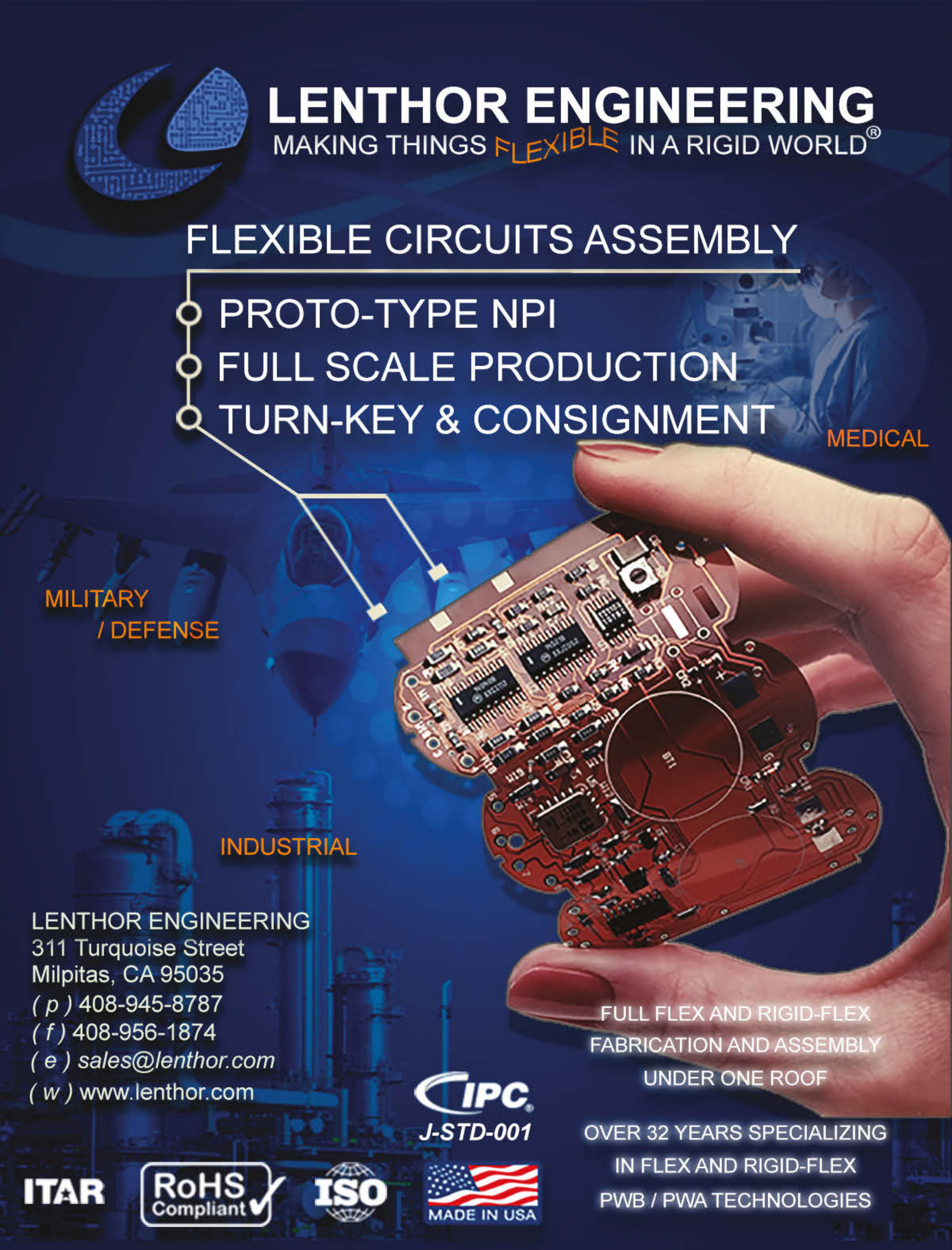
This month, our Flex007 contributors look at which electronic marvels from the original *Star Trek* have come to fruition, which have not, and whether flexible embedded circuits would have been part of the Federation uniforms of 2265. After all, their uniforms did measure and transmit data about each crew member's health—a trick that doesn't seem so far-fetched today.

FLEX007 FEATURE COLUMNS

HIGHLIGHTS

FLEX007 SHORTS

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A Lifetime of Star Trek

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

William Shatner recently celebrated his 90th birthday, and much like the *Star Trek* franchise that he's famous for, Shatner has aged well. No matter how many one-act plays he does on Broadway, he will always be Captain James Tiberius Kirk.

For many of us boomers, it's hard to remember a time before *Star Trek*. I was three years old when *Star Trek* (Original Recipe) came out, and five when it went off the air and into afternoon syndication, so I could watch it after I got home from kindergarten. This was the first show I regularly watched that wasn't a cartoon. Before that, I was strictly a *Flintstones* and *Beany and Cecil* kind of guy.

You must understand: After watching cartoons for my entire short life, *Star Trek* seemed like reality. I didn't see special effects. To me, this was the exciting, real world outside of Cheverly, Maryland.

Beam me up, Scotty! Kindergarten wasn't cutting it for me, and I didn't like listening to my parents. Dad was always discouraging me from doing things that five-year-old boys naturally want to do, like hitting bullets with a hammer. What a party-pooper!

I knew my dad was somewhat cool because he was taller than my friends' dads. But as a mere chemical engineer, he wasn't nearly as cool as Kirk—a father figure managing a quirky

Andy as a toddler roughhousing with his dad.

group of crew members. Unlike my dad, Kirk always wore a cool uniform, not a pocket protector. Kirk was (almost) always in control, whether flying through space at warp speed or exploring some alien planet that just happened to have the same oxygen makeup as Earth.

Star Trek taught us a lot of life lessons. For many of us, it was our first glimpse of what it's like working in a team environment. Each episode taught us about cooperation, putting the group's needs above that of the individual, and knowing when it's time to put everything on the line. And with the red-shirted crewmen, we learned that sometimes bad things happen to good people.

But by far, the best thing about *Star Trek* was the technology. One day, I told my dad, "The transporter on *Star Trek* made a guy disappear! Can we get a transporter?"

My dad broke the bad news. "It's just a TV show. We can't really do that, and we probably never will. And don't try to build a transporter or hit bullets with a hammer."

And then there was the communicator, the coolest walkie talkie ever, and certainly the best handheld prop on the show. When you bought your first clamshell phone 20 years ago, didn't you try to flip it open like Captain Kirk? I guarantee that when Martin Cooper made the world's first cellphone call on the Motorola DynaTAC 8000X in 1973, he was thinking, "How soon until we can shrink these down into the size of Kirk's communicator?"

So, this month, we're helping Shatner celebrate his 90th birthday with an issue devoted to *Star Trek*. In this issue, our Trekkie contributors delve into the technological marvels introduced on the show, and take a look at how far PCB design and manufacturing technology has come since that first episode, "The Man Trap," debuted in 1966, winning its time slot in the Nielsen ratings.

We've even rewritten the show's preamble, which forms a theme for this special issue:

Space and trace, the final frontier.
These are the voyages of the PCB designer.
Their ongoing mission:
To explore strange new vias...
To seek out land patterns...
And new base materials.
To boldly go...
where no PCB designer has gone before!

In this issue, we bring you a variety of articles and columns that pay homage to *Star Trek,* written by expert contributors Happy Holden, Clyde Coombs, Cherie Litson, Dana Korf, Joe Fjelstad, Alun Morgan, Alex Belelovsky, John Talbot, and Matt Stevenson. We also have columns from our regular contributors Barry Olney, John Watson, John Coonrod, Kelly Dack, Tara Dunn, Vern Solberg, Patrick Crawford, and Jade Bridges. And this month, we introduce a new series by Anaya Vardya, DFM 101.

Summer is here, and it looks like we're getting back to some semblance of normalcy. Let's hope! See you next month. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking here.

Star Trek, the Original Series: An Homage from a Fan

Feature Article by Happy Holden
I-CONNECT007

It's fun to think back to the days when I first saw *Star Trek* on TV. In September 1966, I was a sophomore in college, studying chemical engineering. As a science fiction fan for many years, I was excited about this new show, so I would get to the student union building early in order to get a seat in the TV room. I got interested in science fiction from a few good movies like *20,000 Leagues Under the Sea* (1954) and *Forbidden Planet* (1956). Then I took up reading the magazine *Scientific American* at the library. Many a night, after listening to my favorite radio programs (we did not own a TV in 1954), I would walk to the public library and check out the classic science fiction books by H.G. Wells or Jules Verne, among others (Figure 1).

Figure 1: From elementary school until college, most of my science fiction was a few good movies and the classic SF books from the masters.


Hmm, what is the difference between **base and finished copper weights?**

Viewing *Star Trek* for the first time as a 19-year-old was a far different experience than viewing it years later as reruns, especially after 1977, when Lucas brought out *Star Wars*. The special effects in *Star Wars* changed your perspective, even if the story line was still "cowboys and Indians in space."

Even before college, my interest in electronics had grown through building my own shortwave radio (Figure 2). In San Diego, where I attended public school, it was required to take both wood shop and graphics arts (drafting and photography) in middle school. In eighth grade, I took metal shop (fabrication and welding) and electrical/electronics shop (electrical fundamentals and basic electronics). It was all from the perspective of hands-on, handcrafted wiring.

To pay for my education, in addition to scholarships, I worked part time as a lab tech in the Geophysics/Oceanography Department at Oregon State University. This involved field paleo-magnetic/gravity surveys and ocean patrols on the university's exploration ship. During this period, my high school friends wrote a time-share program for the university's CDC-6600 and thus every student now had access to BASIC and Fortran. The university sold this software to Control Data for a new CYBER-70 and the computer department expanded its DEC PDP-8 to now handle nearly 2,000 nodes. In 1968, I moved up to a job as the electronics tech for the psychology department. This was my introduction to military surplus, as the university personnel would drive 45 minutes north to Salem and pick over old and excess military gear.

Since they were tearing down the old IBM-based SAGE Early Warning System, there were vast quantities of electronics and components available to salvage for student laboratories. Old blood plasma containers made perfect Skinner boxes (once I had modified them). Also in 1968, the psychology department received a $8,300 NSF grant for a new DEC PDP 8/L minicomputer for the student labs (Figure 3). That would be equivalent to about $86,000 today. It was my job to design

Figure 2: I received an Allied three-band shortwave radio kit for Christmas in 1959 and wired it up myself. From then on, I bought kits from HeathKit or Eico, including a new color TV kit after I joined Hewlett-Packard in 1970. *Star Trek* had been cancelled by then.

Figure 3: The digital PDP 8/L was the latest in 12-bit minicomputers. You had to manually toggle in the RIM Boot Loader with its front-panel switches so it could read a paper tape for the program from the ASR-35 teletypewriter. All the PCBs were single- and double-sided NPTHs with a wire-wrap backplane.

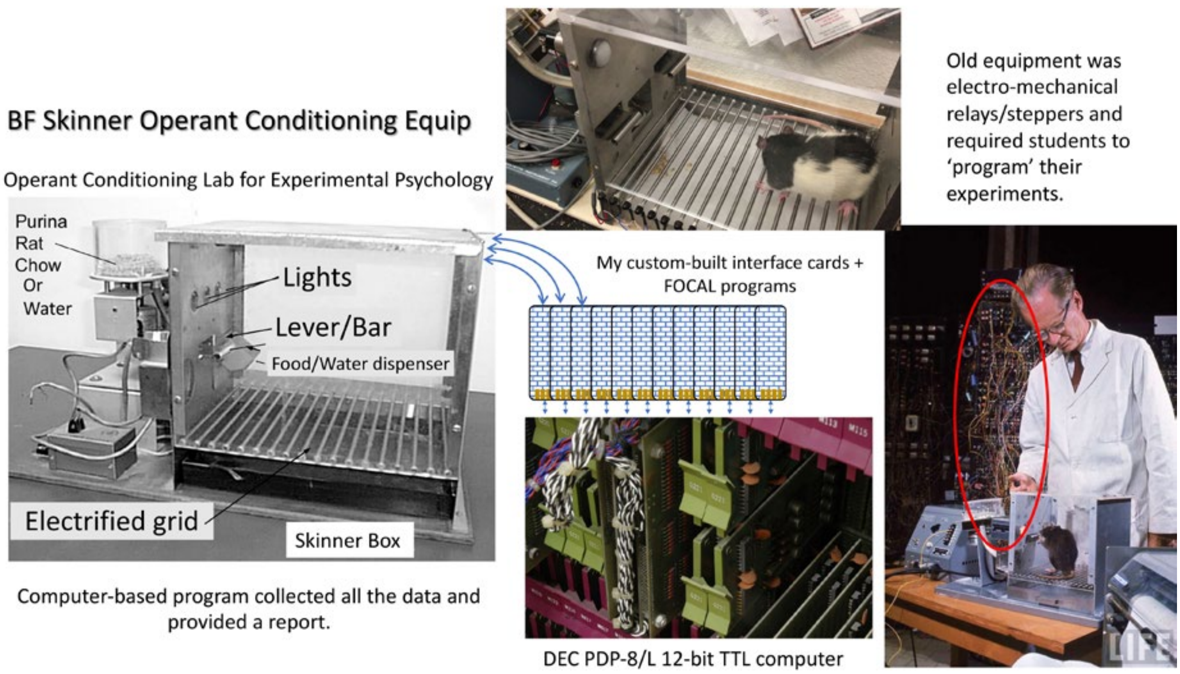


Figure 4: The food sensor-equipped Skinner boxes used for experiments on rats were interfaced via custom PCBs to the new DEC PDP 8/L minicomputer, replacing the old electro-mechanical steppers and relays that were unreliable and difficult for students to program.

the interfaces for the Skinner boxes I had built and program the computer to replace the old electro-mechanical steppers and relays that had previously powered the lab.

The electro-mechanical patch panels were always breaking down and were unreliable, as well as being impossible for most of the students to program (Figure 4).

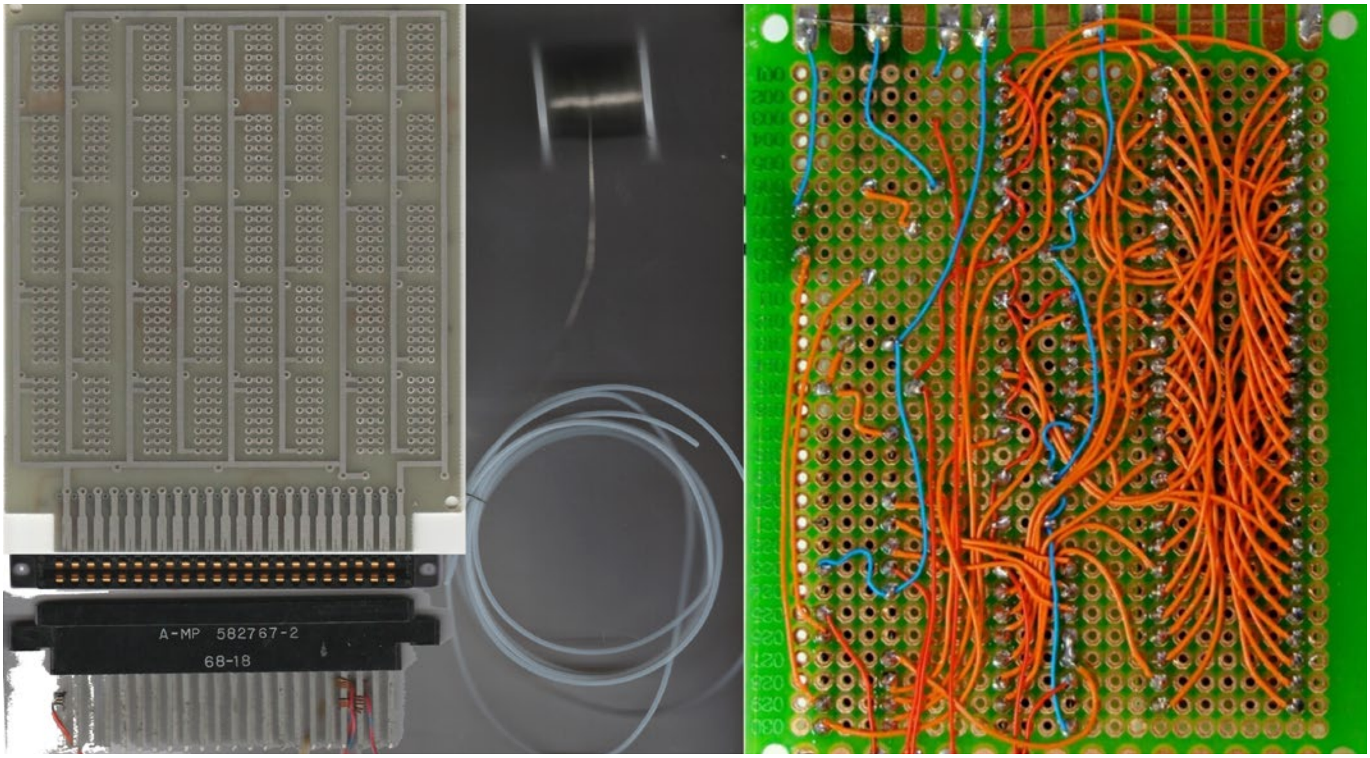


Figure 5: Bare tin-lead breadboards were manually wired with tin-coated copper wire and insulators for all the custom electronics, even by the electrical engineering and computer science departments.

Video 1: The DEC PDP 8/L. Click here to view video.

Video 2: The DEC PDP 8/L. Click here to view video.

This new DEC computer featured printed circuits that were all single-sided or double-sided, non-plated through-holes (Figure 3). I did not know anything about PCBs at the time, so I followed the computer science department and used their tin-lead plated, NPTH breadboards to wire up my new computer interfaces with component drivers (Figure 4). Sockets were used for the integrated circuits and the wiring was done with solid tinned-copper wire insulated with PTFE tubing (Figure 5). No one said a thing about the connector fingers being tin-lead, and that if plugged into gold bifurcated connectors, a galvanic corrosion would be set up.

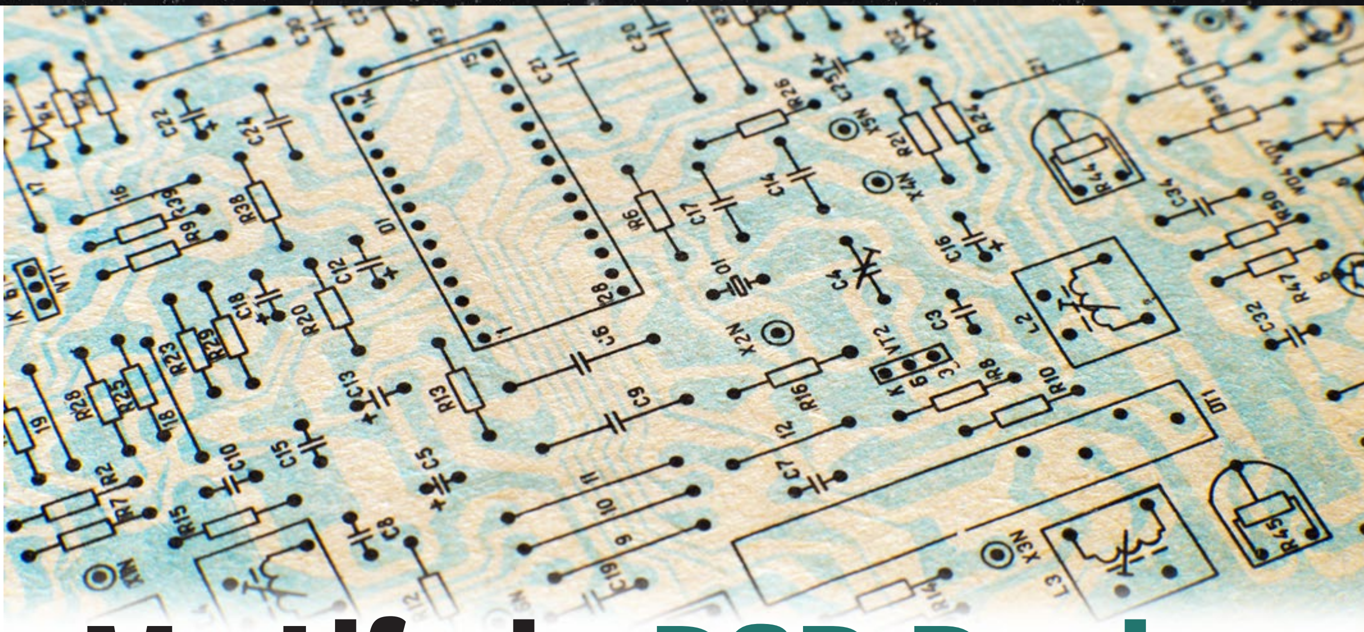
So, it was a common practice to remove all the PCBs and vigorously "erase" the fingers with a pink gum eraser to remove the corrosion products. This was especially important as the students' rats were housed in the closet near the computer and you could always detect the faint smell of urine in the air.

Later, after joining HP, I learned about printed circuit fabrication and designed the artwork for new interface cards. I had them made as PTHs in our Palo Alto, Calif., PCB facility and assembled with proper wave soldering. I sent these back to the psychology department and instructed them to remove my old hand-wired boards and use these proper boards instead.

Years later, friends tell me the old blood storage Skinner boxes and PDP 8/L computer are still there working fine. I wonder if they updated any of my programs?

It's been a long time since *Star Trek* debuted, but I expect technology to continue to go where no designer has gone before. **DESIGN007**

Happy Holden has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa/Westwood, Merix, Foxconn and Gentex. He is currently a contributing technical editor with I-Connect007.



My Life in PCB Design

Feature Article by Cherie Litson, CID+
LITSON1 CONSULTING

Star Date 1978

"Change is the essential process of all existence."
—Science Officer Spock

In a cold (62°F), semi-dark room, there are banks of mainframe computers along one wall; a soft light glows upward from the table in the corner. I take my kit—a variety of sizes of black, red, and blue tape, decals, and an X-Acto knife—and set it on the side table. On the top edge of the light table is a bar with pegs spaced about eight inches apart. A sheet of Mylar imprinted with a 1/10th-inch grid is fitted over the pegs and taped down in the corners so it won't move. On top of this are two sheets of clear Mylar—one for the two sides of traces and one for the pad master of the circuit board I'm creating. Later, I'll add another sheet for all the reference designators and part outlines. I have some decals for those, too.

This is the first board I get to do myself from start to finish. I've been apprenticing for three years now. I've been drawing all the schematics from napkins and scraps of notepaper from the engineers, creating the sepias for the fabrication and assembly drawings, and being the gofer running all the files around to the photoshop and fab house. I have an engineer-approved schematic and I've made a rough sketch of where I want to place each part and the connections between them. Today, I start placing the decals and tape.

I have to wear a warm jacket and hat in this room as I carefully place each component decal (most are 14-pin DIPs, resistors, caps, and a few transistor cans) on the intersections of the grid lines and carefully align them to each other. Once I put them down, I don't want to move them as they won't stick so well then. This layout will be the typical 4:1 scale, so I need to place my targets outside the board for the photographer to sight on when they reduce the artwork. This is how we've been doing PCBs since the '60s.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IN OUR DUST BY INVESTING
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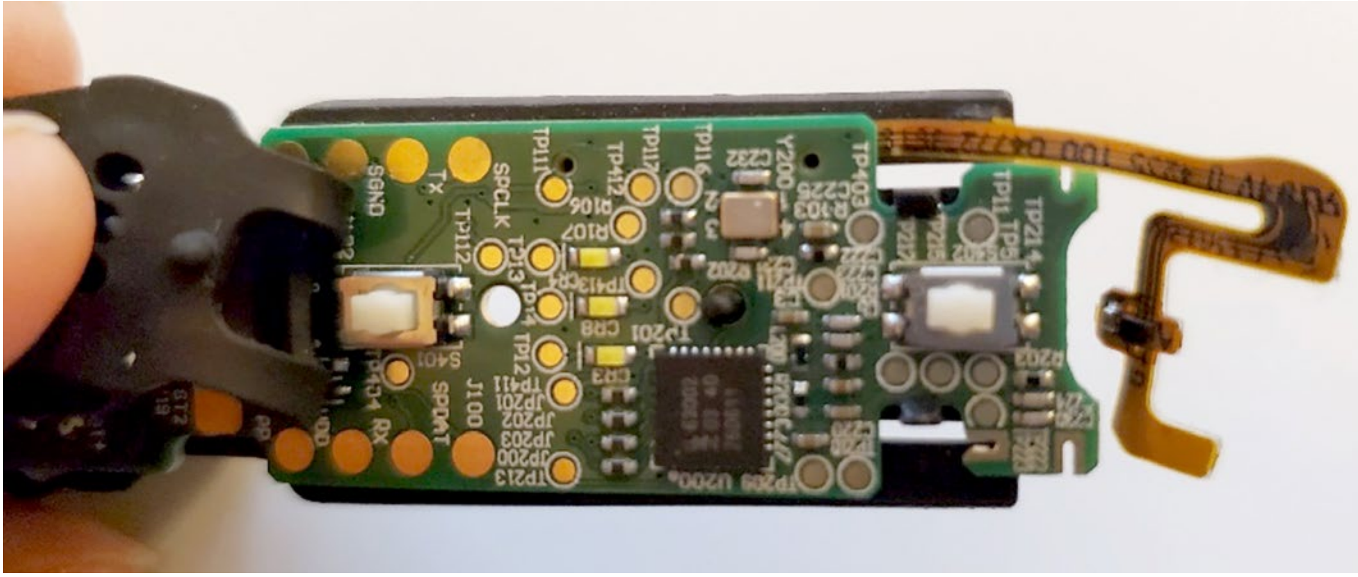


Figure 1: 2008–2018 era: Philips electronic toothbrush.

Star Date 1988

"We prefer to help ourselves. We make mistakes, but we're human—and maybe that's the word that best explains us."

—Captain James T. Kirk

Now in the late 1980s, there's this new method for designing PCBs. I've looked at it. It's a new software program called OrCAD that lets me export this file—ASCII, I believe—that has all the connections from the schematic, and then import this to the graphic layout portion of the program. This is a great time-saver, especially for doing the schematics and pre-sketch of my boards. It's a little slow on my new 286 computer because it uses a lot more memory space than AutoCAD does. Also, I can't get a good printout with the dot matrix printers for our photographers. The image is too grainy, even when reduced. Guess I'll still need to do a tape-up of the boards. Glad I got my EET degree, though, as these layouts are getting tougher. I keep getting asked if I know how to do a twisted pair on a circuit board. Don't know if that's even possible yet. And it would take up a lot of real estate to do something like that.

Finally! We got new inkjet plotters that create an image that can be photographically reduced. It's a bit of a slow method and we have to run the plotter overnight for some of the larger jobs. When no one is around, unfortunate events will happen. One design got totally stuck printing one hole pad many times over and made a mess of the plotter. Have to be careful not to put down multiple pads in one location as those plotters are expensive. But it sure makes great plots of schematics, and doing changes to the design are much easier now.

Star Date 1998

"I'm a doctor, not a physicist!"

—Dr. "Bones" McCoy

I'm a designer, not an engineer! Oh wait; I am an engineer now. I'm working with the Microsoft hardware team for mice, gaming, and keyboards. Good team of layout people we have here. I love the new software programs I'm learning—P-CAD, Protel, more OrCAD, and PADS. I've been learning a lot about mass production from Tim Bucwalter. One of our other co-workers, LaVern Mullet, asks if I want to go check out this PCB design course. They are going to have a three-day workshop next week and we could sign up for it now as they have a few spots open. Some guy named Dieter Bergman is going to be teaching it and he's supposed to know a lot about PCB design.

Then we can take this test and get a certification. Sounds good to me. Tim doesn't want to go, so just LaVern and I go. What a surprise that was. I barely passed that exam. There's this whole world of manufacturing protocols that I had no idea existed. I need to know more.

Star Date 2008

"I canna' change the laws of physics."
—Montgomery "Scotty" Scott

After an orbit around the planet to conventions, fabrication shops, and manufacturing shows from the U.S. to Italy, China, and back, I've managed to become aware of just how large the universe of PCB design has become and how much more I have to learn. I've managed to bring a few other designers along with me after starting our Cascade IPC Designers Council Chapter, taking the CID+ course, and becoming a CID instructor. Chapter meetings and presentations are helping us discover new ways to do layouts and make great contacts with other people in the field. Differential pairs, microvias, special materials, surface mount components that get smaller and smaller each year—these changes keep happening so fast. Now, 3D

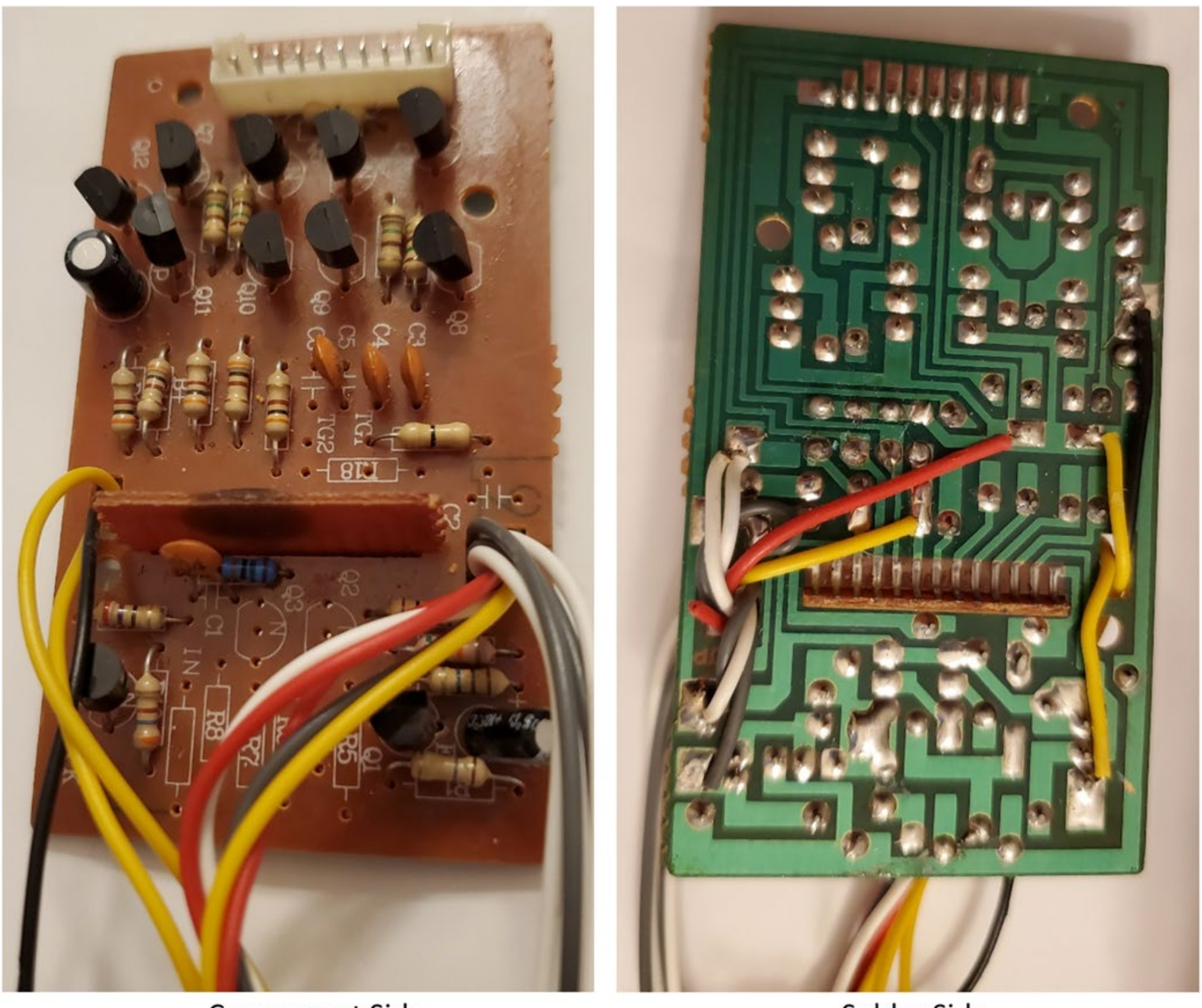


Figure 2: 1978–1988 era: single sided board with additional board soldered on as a connector (similar to what I did then.)

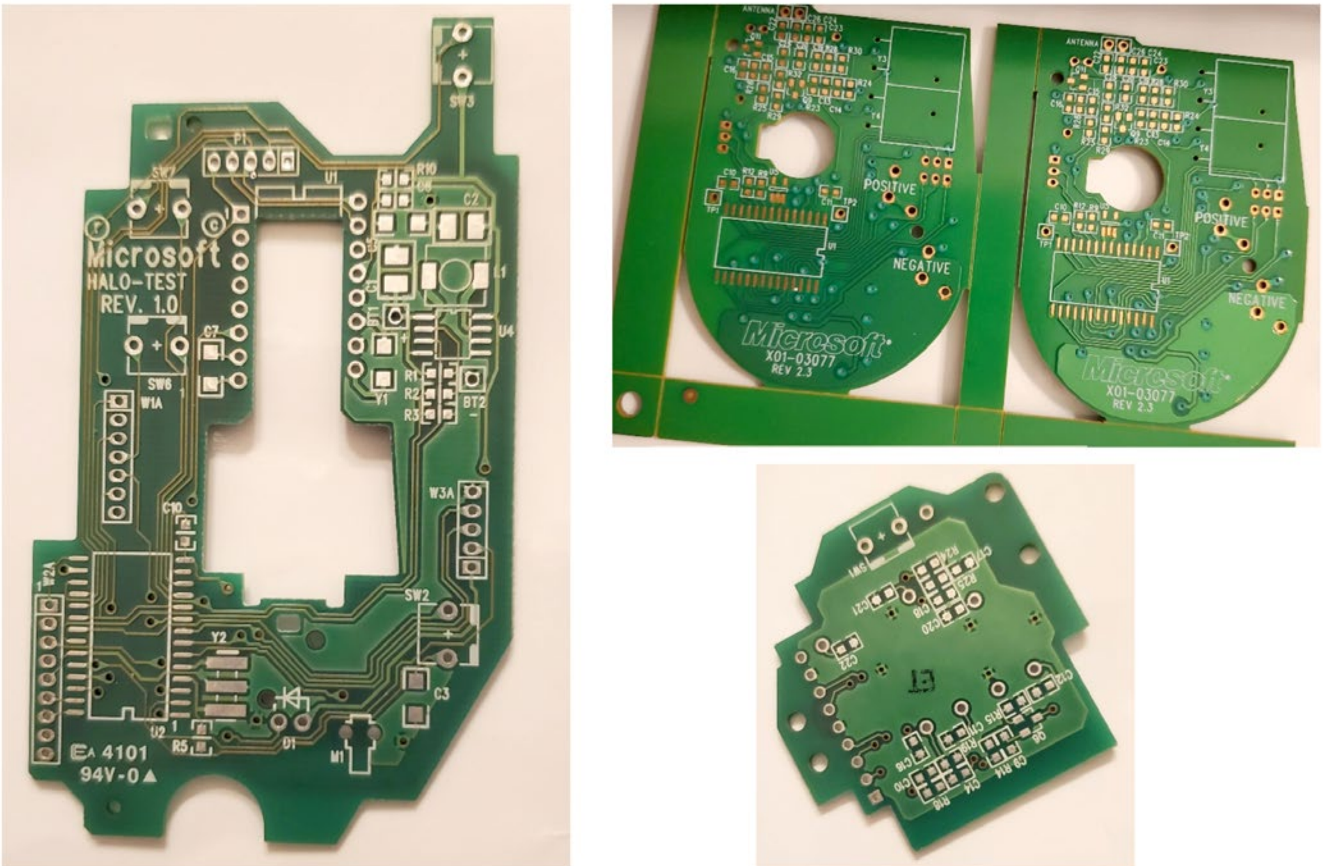


Figure 3: 1998–2008 era: wireless mouse and trackball.

design integration is really the bomb. We all need to start using this.

Later, we lost some great people in our industry—Dieter Bergman and Glenn Wells among them. Many others have retired or moved on to other ventures during the financial downturn. I'm now a certified instructor for the CID program and am more involved with standards. Also, I'm starting my new career path as a freelance designer.

Gary Ferrari is connecting me and the other instructors with EPTAC, and now I'm one of the CID/CID+ master instructors. That also includes being on the IPC Executive Board. We're rewriting the CID and CID+ to update some of the material and add in HDI and flex circuit design. I'm tasked with compiling the CID material. IPC wants us to do the exams online, but we haven't seen software that will support that with the level of integrity we need. Someday it will happen.

Star Date 2020

"One man cannot summon the future."
—Spock

"But one man can change the present!"
—Kirk

What a crazy decade this is. IPC is changing its focus for design and manufacturing education to the college level. We've seen the beginning of the Printed Circuit Engineering Association (PCEA) to support the professional engineers already in the workforce. The COVID-19 pandemic is impacting the supply chain. Online webinars, magazines, and trainings are on demand everywhere. More companies are now okay with remote workers, and many even encourage it. Zoom is making a big impact. Global political upheaval is creating uncertainty with everyone. Electronic everything is being developed—from cars and airplanes to communication and space exploration. Design engineers are becoming the most sought-after technologists in the industry. We have new ways to manufacture fine lines to fit the components and keep up with the speed of the circuits. Flex designs are being embedded into clothing and fabrics. Medical breakthroughs are happening with laser technology and artificial 3D printed devices becoming commonplace.

Space is finally being explored once again. Maybe we'll actually venture out to other planets, both within our solar system and beyond. Hopefully, this will happen before I hit 100 years old. But I hope to be designing boards until then.

Star Date 2028

"There is a way out of every box, a solution to every puzzle; it's just a matter of finding it."
—Captain Jean-Luc Picard **DESIGN007**

Cherie Litson is an instructor at Everett Community College in Lynnwood, Washington.

Hate PCB Respins?

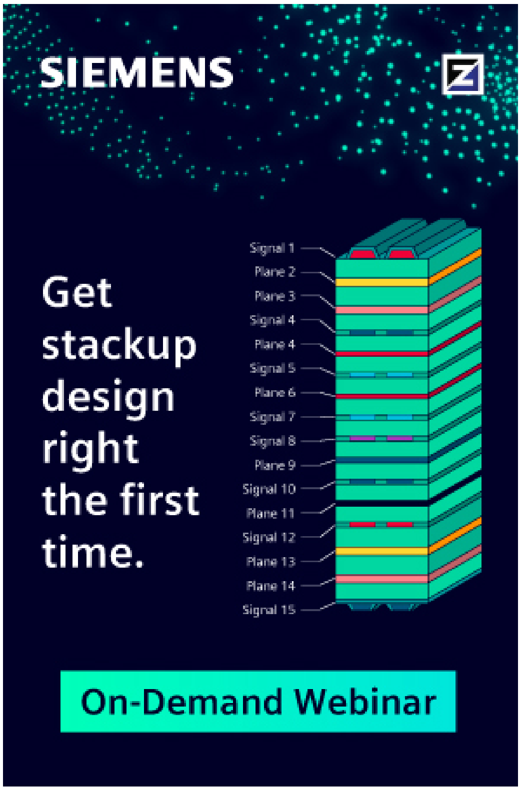
Five Ways to Reduce or Eliminate Respins

Patrick McGoff

Redesigning a printed circuit board is a chore that no one likes. Respins of printed circuit boards cost money, delay the schedule, and just aren't enjoyable for anyone. Yet, many companies are not taking advantage of available tools that can reduce—and in many cases eliminate—PCB respins. Instead, issues that make the PCB difficult or impossible to manufacture are found late in the process, even by the fabricator or assembler. The later in the process, the greater the cost to fix—and it's not linear.

There are many causes that commonly result in a board that is either impossible to fabricate or assemble, or would produce such a small yield that the cost would be out of range. Whenever this happens, the board must be redesigned to correct the problem before manufacturing can commence.

Often issues are not caught early because of lack of insight to the fabrication/assembly process, and inability to detect the problems visually. A design may appear to meet specs for trace width, but a particular manufacturer may not be able to maintain a minimal-width trace due to undercutting. This is something that would not normally be in a PCB designer's realm of knowledge.



The key to avoiding respins is to employ design for manufacturing (DFM) techniques, not just before releasing to manufacturing, but all throughout the product design and creation process. Here are five ways that DFM can help you reduce or even eliminate PCB respins by employing Siemens PCB DFM solutions.

Every PCB design begins with a stackup. The top and bottom must be aligned as well as any signal and planes in a multilayer board. Stackup issues are one of the top reasons that respins are required. With higher and higher edge rates, material selection becomes more critical. The traditional methods of using a spreadsheet to define the stackup has run out of gas for today's speeds. To read this entire article, click here.

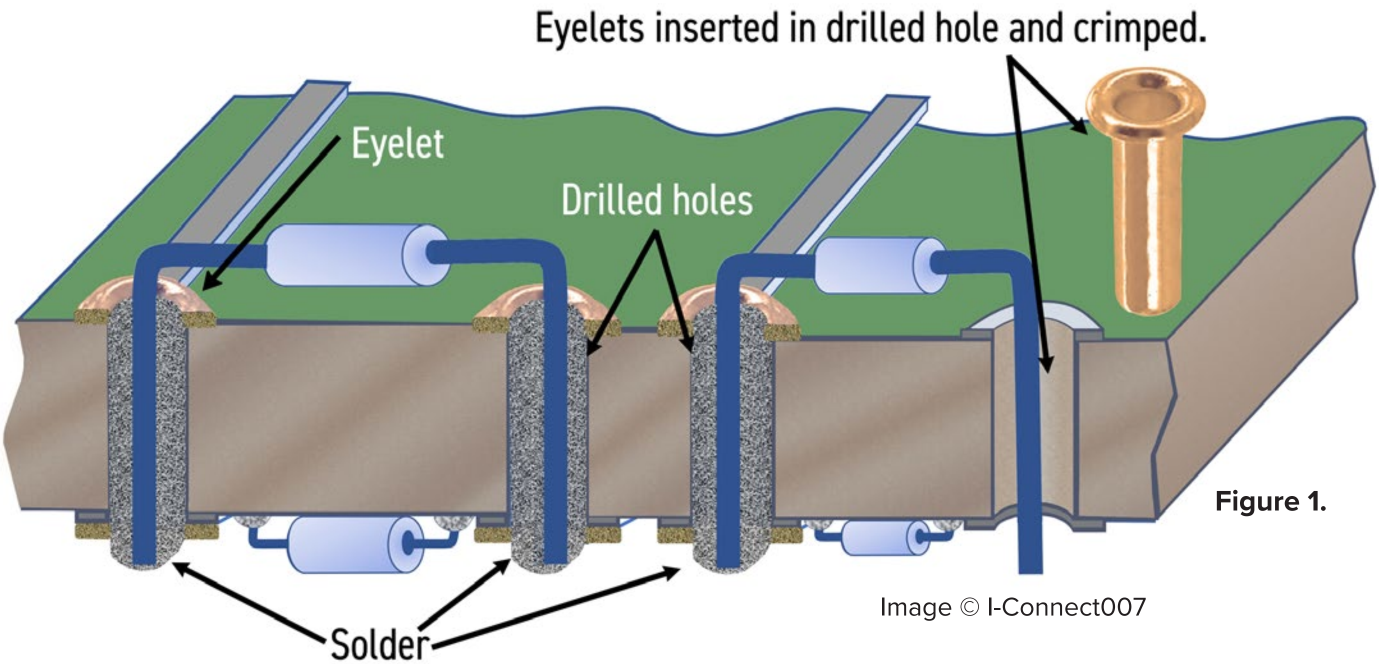


Figure 1.

Image © I-Connect007

Hewlett-Packard's Adoption—and Controversy—of Plated Through-Holes

Feature Article by Clyde Coombs

In this issue of *Design007 Magazine,* we're taking time to reflect on the development of PCB technology since the first episode of *Star Trek* aired in 1966. I believe that it is instructive to remember just how close Hewlett-Packard—and likely the entire industry—came to adopting eyelets instead of plated through-holes in the early 1960s.

Except for the transistor, no other technical development of the 20th century has had such a profound impact on all aspects of daily life as the plated-through-hole (PTH) printed circuit. In its role of interconnecting digital components reliably, cheaply, and universally, it makes possible all the wonders of modern life that utilize the transistor.

That there was ever a controversy over the use of plated through-holes as an acceptable printed circuit interconnection process seems almost impossible to consider, let alone take seriously today. But in the late 1950s and early 1960s, the PTH was not just a controversial

Figure 1 above: The image shows a cross-section of a typical double-sided eyeleted PCB in the late 1950s. Each side of the board has been laminated with copper. The board has had etch resist printed on the copper with the silkscreen process, and then, typically, etched in ferric chloride. After the resist is removed, holes are drilled and the board is ready for the eyelet process. Eyelet machines were the same machines used to put eyelets in shoes. Eyelets were installed one at a time by positioning a hole in the board onto the anvil of the foot-activated eyelet machine. The machine would insert an eyelet as shown, shaped by the anvil to produce either a crimped form or—in the case of single-sided boards—a flared form to capture more solder on that side. The eyelet then provided the metal contact between the two sides of the board, and the significant metal barrel allowed the solder to provide electrical connection and physical support for the component lead.

idea; serious product designers considered eyelets a preferred technology. It became a competition, and people took sides. It was a slow week if *Electronic News,* a very important industry publication at the time, did not print an article reporting a new study, or just quoted a learned opinion, on the benefits or perils of one versus the other.

Hewlett-Packard was not immune to this controversy at the time. In 1959, HP was still recovering from the misuse of single-sided boards in a new product. The poor reliability of that instrument had not only done serious damage to the company's credibility on quality and reliability, but had caused serious financial issues on rework, repairs, and lost sales. At this point in time, major electronics companies such as Sylvania Television and Tektronix Instruments were actually advertising that their products did not use printed circuits. In response to this problem, HP had turned to eyelets to solve the immediate issues, and that did have a benefit for those single-sided boards. A bigger problem, however, was looming as all the new products were to be designed with transistors, which meant that both sides of a board would be needed.

Young Engineer, Risky Project

That's when, and where, I came in. I was a newly hired electrical engineer tasked with bringing the company into a printed circuit technology that would be an advantage to the product and perceived as such by the customer. To illustrate the level of misunderstanding of the real problem, it was viewed as an electrical engineering issue because it was dealing with interconnecting electronic components and circuits rather than the mostly chemical engineering challenge that I soon found it to be. They had the wrong person. However, I had the job.

After some stress tests on both eyelet boards and plated through-hole sample boards, I became convinced that the only process that could achieve company reliability and cost goals was the plated through-hole. Getting others at the company to agree with me, even given my test results, was a much bigger problem than I ever imagined. Coming off the previous experience with printed circuits, product engineers did not want to abandon eyelets, since they were now working, and insisted on refining that process to the new double-sided need. Their argument was, basically, that "plated through-hole" was absurd on the face of it. How could any reasonably sane person expect to plate copper in hundreds of small holes, drilled in a nonconductive material, and not have many fails? I actually had three senior technologists each provide me with information on separate eyelet processes they insisted would work.

One thing they did not seem to remember was a basic physics issue: brass eyelets and epoxy-based PCBs have a different co-efficient of thermal expansion. Intimate contact between the two after soldering was mostly lost, leaving the solder to provide the connection between them, causing all the touch-up and rework we were experiencing in production. One product manager was so alarmed by my advocacy of plating that he went to Dave Packard personally and demanded that I be fired before I destroyed the company.

Packard was well aware of the company's commitment to transistorized products, and the resulting reliance on printed circuits, so he asked me to give him a personal review of where we were on a workable process. I spent two hours explaining that what I was proposing was not "black magic" or an "art," but was based on a chemistry that could be readily understood, controlled, and predicted. To show that it would work, I had two sample boards from new instruments that the product designers had agreed to include. He was convinced and signed off on the budget for the first shop: $25,500. To be fair, we did not need a new building, as I was able to use the space that had been made available when the general plating shop was moved to a bigger facility.

Getting to the point where the review with Packard was possible took almost two years. To start, the only electroless copper deposition process I could find was a product called CopperCold, which was basically unstable. When successful, there would be copper in the hole that provided a conductive surface for electroplating the copper for the circuit; however, it left an interface between the base and deposited copper that required mechanical removal to ensure a reliable circuit. When it was not successful, it caused all the copper to drop out of solution at once.

Shipley's Gene Weiner to the Rescue

In early 1960, I had been working with CopperCold for some time, and all I was getting was puddles of copper at the bottom of the tank. Out of nowhere, I got a call from the HP lobby informing me that there was a representative of a company called Shipley waiting to see me. I met the rep, Gene Weiner, who introduced himself and said he was there to solve all my plated through-hole deposition problems. I thought, "Yeah, right!"

He said he had heard HP wanted to get into the plated through-hole business. He set up a miniature deposition line on my engineering bench and asked for a sample of the double-sided copper clad material we were using. He then proceeded to blow me away. It worked! I would do considerable testing on the deposited copper and its adherence to the base material, and I couldn't find any problems. So, I got Gene a purchase order, gathered all the CopperCold materials for disposal, and never looked back. Gene left and I didn't see him again for almost 20 years. It was like the Lone Ranger coming out of nowhere, solving the problem, and then riding off. (Who was that masked man?)

The Shipley patented process had the ability to control the deposition of copper and create a structure that bonded with the base copper. Although some shops continued to remove the copper deposited on the surface, we at HP didn't have the need for that step.

Copper deposition was the key step, but other steps presented their own problems. For example, it was common to panel-plate copper to the board and then apply a resist to the circuit pattern and etch away all the exposed copper. In addition, the standard copper plating solution was acid based and plated about twice as much copper on the surface as it did in the hole.

An alternative process using pyrophosphate was a pH-basic solution and more difficult to control, but it plated much less copper on the surface for a given amount in the hole. The problem, besides control, was that a silkscreen resist of the day did not survive the high pH. We worked with a resist supplier to develop an appropriate resist and we were able to develop a process that would pattern-plate copper, put up to two mils of copper in the hole, and reduce our waste copper by about two thirds. I wrote a paper showing the total destruction of a board with a soldering iron but leaving the plated hole and attached circuitry still intact in its original form.

Since I was learning as I went, when I had

my meeting with Packard, I had not yet developed a tin-lead plating process to be used as an etch resist on the traces after copper plating. I used gold, which, although expensive, solved the short-term problem in developing the copper plating step. Solder would get its turn. So, the boards Packard saw were gold-plated, but I had a schedule to show our goal of replacing it with solder. However, before I got to that item on my agenda (but after he had had the boards in hand for some time), he asked me how much gold was on the board (remember that this was 1961 and gold cost $35 an ounce). I told him, and before I could bring up the solder (tin-lead) plate plan, he commented that that didn't seem too much, and it gave the board a look of quality.

Packard said, "When you buy HP products you should get quality and it should look like quality." I never did learn to plate solder. And HP boards became famous (or notorious) for the use of gold for years to come.

When the two instruments with plated through-holes went into production, not only did they have double-sided capabilities, but eliminated all the problems of eyelets such as insertion of the eyelets, touch-up and repair of discontinuities at the eyelet, and resilience to repair in the field, and passed all stress tests without one board-related issue. The result was a complete reversal of opinion among product managers and a stampede to use plated through-holes in all new products and to convert single-sided boards to plated through-holes. Most non-printed circuit, point-to-point soldering techniques were converted to plated through-holes. Within six months, in the middle of 1962, printed circuits were the dominant process and the company no longer required potential new hires to take a company sponsored week-long soldering class as a prerequisite for employment.

The product manager who demanded I be fired never did apologize, and the engineers who had pushed improved eyelet processes never mentioned it again. In addition, 21 eyelet machine operators were reassigned to more interesting jobs.

When I finally saw Gene Weiner again at NEPCON in the 1980s, I was able to thank him for riding to the rescue and making my career in printed circuits possible.

A lot has changed since the 1960s, but it's difficult to believe that our industry was so close to embracing brass eyelets over plated through-holes. I was fortunate to be a driver of HP's move into PTHs, and I appreciate Gene's help in making that process a reality. DESIGN007

Clyde Coombs joined Hewlett-Packard in 1959, where he developed the through-hole process that was the basis of PCB fabrication at HP for over 40 years. He is the editor of all seven editions of the *Printed Circuit Handbook,* with Happy Holden joining him as co-editor of the seventh edition.

‘The Trouble with Tribbles’

Feature Article by Dana Korf
KORF CONSULTANCY LLC

The original *Star Trek* series came into my life in 1966 as I was entering sixth grade. I was fascinated by the technology being used, such as communicators and phasers, and the crazy assortment of humans and aliens in each episode. My favorite episode is “The Trouble with Tribbles,” an episode combining cute Tribbles, science, and good/bad guys—sprinkled with sarcastic humor.

During the second season I started my hobby of repairing and stripping tube TVs and radios in my bedroom for friends and family. These events, along with Mr. Keller’s electricity class I took years later as a senior in high school, started me on my path to becoming an electrical engineer.

Did *Star Trek* subconsciously send me down this path? Who knows? But I have every episode in my video library to this day. It showed us that anything was possible. Little did I know that my venture into electronics, PCB design, and manufacturing would reflect the story’s premise.

These Are the Voyages

One of the first designs that I worked on was replacing a core memory board with those brand-new 16Kx1 dynamic RAM memories from that new startup Micron. For the younger readers, a core memory was composed of a round ferrite core with wires that ran in the X and Y axes with a diagonal wire through the center of the core. A current would run through the X-axis wire to create a “1” state, and the core would rotate until it hit the wires. A current would run through the Y-axis wire to rotate the core to create a “0.” The diagonal wire would put the bit into an indeterminate state. Every morning we would walk into the data center and power up our Data General Nova computer by entering instructions with switches. You knew the system was running when you could hear the cores making a

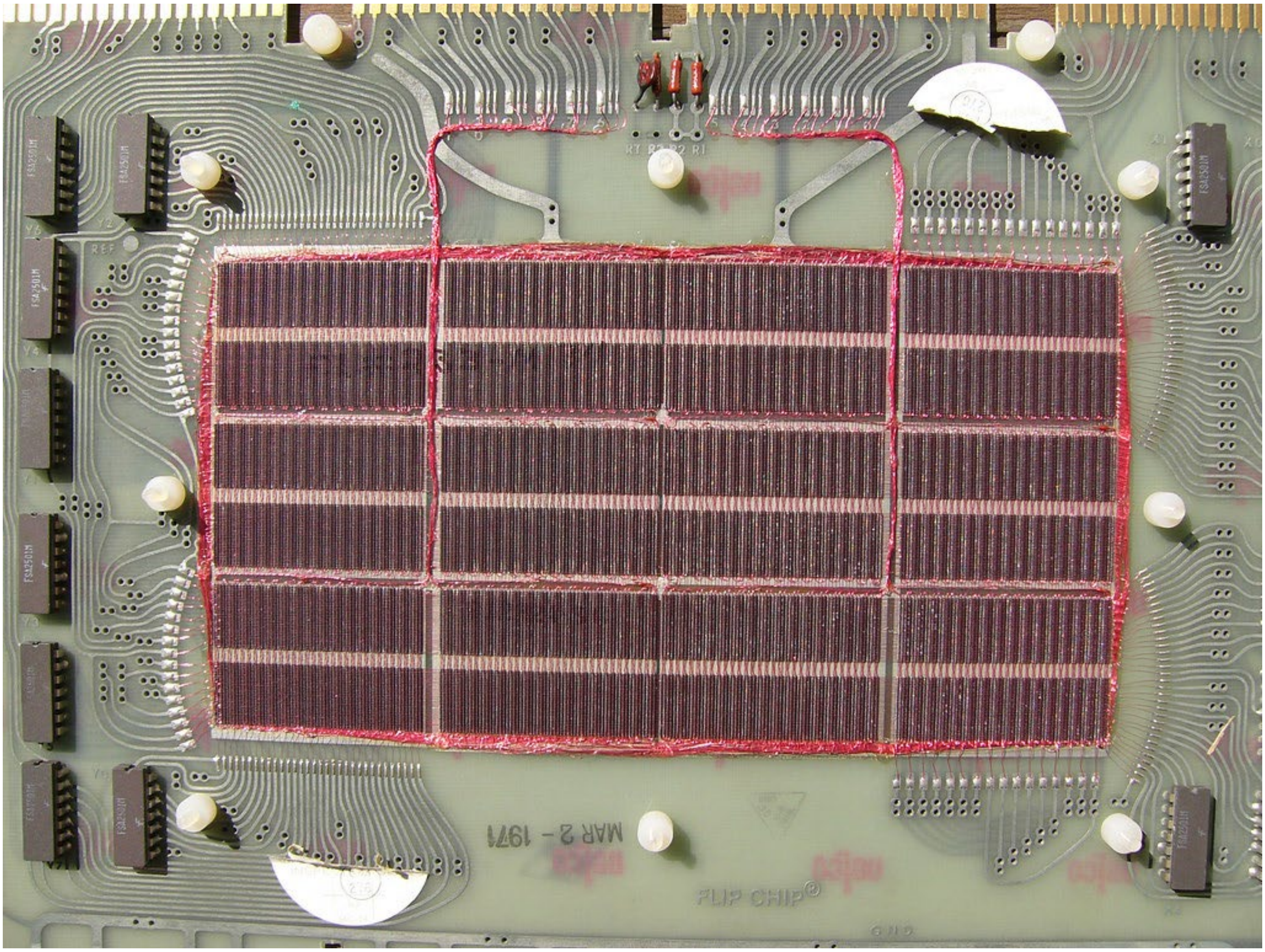


Figure 1: A 1970s core memory board.

specific clicking pattern, like music. Then we would go to our desk and log on to our terminals.

During a final design review of the DRAM-based memory board, the field service engineers were trying to kill the design. The reason presented was, "How can the computer be maintained if a person couldn't hear the memory running?" Fortunately, we won that argument. We had implemented a radically new design just as *Star Trek* used radically new technology.

New design, material development and manufacturing engineers should not be afraid to think outside the box. Western-trained engineers are taught to challenge the norm. But technologists in Asian cultures, unfortunately, often have not been raised to challenge the norm. Hopefully, in one or two generations, they will evolve and be allowed to challenge everything.

Their Ongoing Mission

The PCB industry is generally slow to change. New technologies, materials, and methodologies may take decades to reach full fruition. Here are key opportunities for new engineers to change the status quo:

- Design to manufacturing data transfer: Existing NPI processes assume that the design cannot be built as is. The manufacturer must review all the data (DFM review) to look for documentation errors (conflicting documents), design errors (impedance vs. stackup), and suggest yield improvement adjustments. **Challenge: Build the design as sent to the manufacturer with only process compensation.**

- Intelligent data transfer: Quit using non-intelligent 1960s Gerber-based data with PDF files and move to intelligent data formats such as ODB++ and IPC-2581. **Challenge: The entire industry needs to switch to an intelligent data format.**
- Bi-directional knowledge transfer: Manufacturers need to provide all the design rules, in an automatically loadable format into their customers' CAD systems, that their DFM departments use, so the design can be manufacturable. **Challenge: Manufacturers must provide all design rules and CAD software needs to be modified to use these rules during layout.**
- Material selection: There is a broad array of PCB materials available. There is excellent simulation software that can be used to propose an optimum solution. RF designers may be able to selectively use high-speed digital materials. High speed designers may be able to selectively use RF materials. **Challenge: Look at potential applicability of non-traditional materials.**
- PCB front-end engineering automation: Existing processes assume that humans are required to touch every design to create production tooling. Create fully automated paths to reduce the cost of tooling, reduce cycle times, and improve quality. **Challenge: Use digital twin techniques to create a few fully automated paths.**

Our industry, thanks to the collaboration of organizations like IPC, iNEMI, UL, and HDPUG, has attacked and resolved material, design, and application challenges as they occurred. The industry takes these challenges on in a very professional manner with our customers' safety and product performance in mind.

Significant challenges have been overcome, such as how to connect and reliably solder component pads under devices. We resolved ENIG black pad solderability issues with improved process control. We worked together to determine what materials and material properties were required when we transitioned to lead-free soldering. We have converted the copper trace from just a discrete wire replacement, determined how to create predictable impedances, and learned how to predict insertion loss for that same conductor. Conductors started out on rigid boards, then flexed on flex PCBs which are now being stretched in a random fashion and thrown into washing machines on wearable interconnects. Materials, fabrication, assembly processes, and DFM software tools have evolved to support these requirements.

As the *Star Trek* mission might say, "We will boldly go where no designer has gone before."

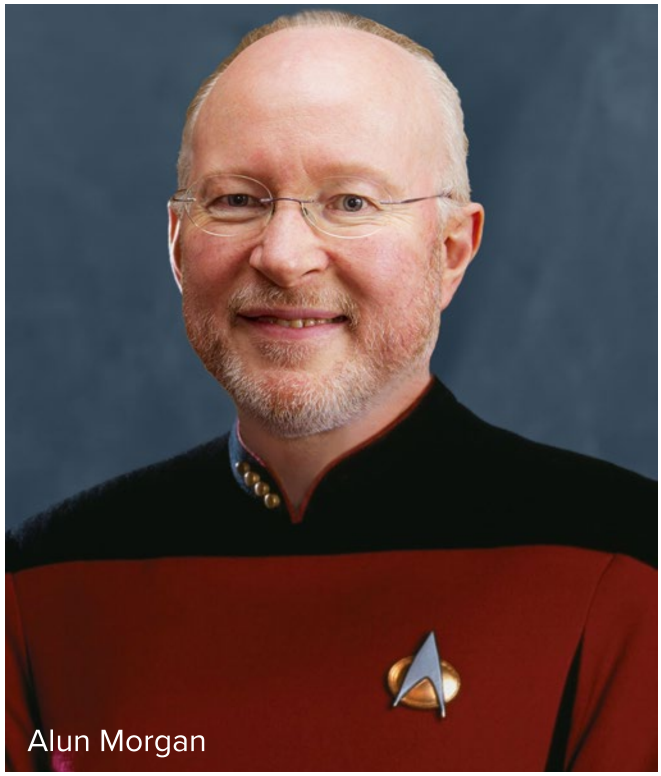
The Blooper Reel

One time when I was in college and attending a free Friday night movie, we were treated to a four-minute clip called *Star Trek Bloopers* which had me crying with laughter. Everyone must see this, as it shows outtakes and specially-added video which I will always remember, especially the final scene. DESIGN007

Dana Korf is principal consultant of Korf Consultancy LLC in Bremerton, Washington, and writes a regular column for I-Connect007. To read past columns or contact Korf, click here.

It's FR-4, Jim, But Not as We Know It!

Feature Article by Alun Morgan
VENTEC INTERNATIONAL GROUP


Alun Morgan

Whilst Gene Roddenberry was writing *Star Trek* in one corner of the U.S., another group of engineers was working on a less daring project, but one which was nonetheless groundbreaking and continues to influence our language to this day.

That group was the National Electrical Manufacturers Association (NEMA), and their magnum opus, at least as far as the PCB industry was concerned, was the "L1" specification. As *Star Trek* was responsible for adding terms such as photon torpedo, dilithium crystal, and warp drive to our language, so NEMA was responsible for the terms G-10, FR-4, and FR-5. "FR" was the NEMA abbreviation for "flame retardant" and materials so classified were marked with a red manufacturer's logo. The terms also marked a change from the early 1960s where materials produced solely from paper reinforcement were used to produce PCBs. NEMA defined the terms used during the transition to glass-reinforced PCB materials that were to become the mainstay of our industry.

The evolution of printed circuit board substrates has necessitated a change of view in how performance is classified. The NEMA classifications are based on the physical properties of the basic chemical makeup of the materials used. We are, for example, used to classifying substrates according to their glass transition temperature, Tg. Accordingly, we refer to "standard," "mid-range" or "high" Tg substrates. It is no surprise, therefore, that many designers and users of PCBs have assumed that the Tg value has a direct relationship to the thermal endurance of the substrate and have specified a "high Tg" product for an application requiring high thermal resistance. I am reminded of Spock's words, "Insufficient facts always invite danger."

The Tg value merely marks a phase change in the resin chemistry whereby enough energy (temperature) is available to increase the rotational freedom of the polymer to allow it to transition from a glassy to a rubbery state. If energy is continued to be applied, then the next transition that would be expected is the Tm, or melting temperature. Here is where thermoset plastics spring a surprise. In theory,

there is indeed a Tm; however, the temperature required to melt a thermoset exceeds the thermal decomposition temperature, Td. The consequence of this is that a thermosetting material never reaches the Tm—it decomposes into carbon and a variety of gases long before it can ever get there. The Tg has no direct correlation with the thermal decomposition temperature.

To specify thermal performance, we need to set our phasers to stun and to consider all performance aspects relevant to the end application. This marks a shift in the classification. It is not sufficient to specify a "high Tg" substrate; instead, performance should be specified according to the application. This may include the Tg, Tm, time to delamination, coefficient of thermal expansion in the Z-axis, and thermal conductivity to fully characterize a substrate suitable for applications requiring a focus on thermal management.

To specify thermal performance, we need to set our phasers to stun and to consider all performance aspects relevant to the end application.

Since the days of *Star Trek,* we have also moved from impulse power, and believe it or not, my first job after leaving university was in a research laboratory where a space impulse engine was developed to "warp speed." I am, of course, referring to the continuing journey of increasing signal speeds and data rates. James Montgomery Scott (Scotty) famously said, "I canna' change the laws of physics." So far as we know, he was correct; however, we can certainly exploit them.

The PCB world of the 1960s was a much simpler place. Our reference frequency was 1 MHz and circuits were largely comprised of analogue devices, with very few of the nasty square waveforms with theoretical bandwidths tending toward infinity to deal with. The high-frequency spectrum in the past was divided into two bands—one where FR-4 worked and one where it didn't. Where it didn't, many designers faced a no-win scenario where they couldn't use FR-4 and the only alternative was PTFE which could push the project into an insurmountable position of unaffordable cost and limited materials availability.

When Captain James T. Kirk faced his no-win scenario in the simulated encounter with the Klingons in "The Kobayashi Maru," his solution was to cheat. Circuit designers today are indeed fortunate that they have no need to cheat as the gap between FR-4 and PTFE performance and cost has been filled by entirely new ranges of substrate materials based on their performance at high frequency and high data rates for digital circuity. These new generations of material allow the designer the flexibility to select the appropriate substrate for the application without over-engineering performance that is neither required nor can be afforded.

FR-4 itself has also evolved. In the 1960s, it was a single grade, but today it encompasses a range of materials with diverse properties and chemistries. The recent split into FR-4.0 and FR-4.1 (characterizing brominated and non-brominated flame retardants, respectively) came about in recognition of the fact that all FR-4s do not perform the same and test results of one variant could no longer be considered representative of another. "It's FR-4 Jim, but not as we know it!"

Despite the recent years of tremendous upheaval in our industry, I hope that you share my enthusiasm and excitement for our continuing mission to aggressively seek out and develop the material solutions of tomorrow. May we all live long and prosper as we boldly go where no one has gone before. **DESIGN007**

Alun Morgan is technology ambassador for the Ventec International Group.

There is No 'Final' Frontier for PCB Design

Connect the Dots

Feature Column by Matt Stevenson, SUNSTONE CIRCUITS

Methods may have changed, but the goal for PCB designers remains the same: create better PCB designs, always seeking to improve everything from manufacturability to durability. We must keep up with the latest CAD tool features, choosing the right design tool for your design. As the design and manufacturing process evolves, we must grow in our understanding.

The tools we use for PCB design have changed a lot since the USS Enterprise went on its first mission in 1966. We all remember the cardboard sets and ridiculously tight shirts from the original show, but how often do we think about what the crew could make that ship do from a bridge with fewer instruments than a toddler's first cash register?

Sulu did a lot with not much. He was flying that baby at warp speed, then stopping on a dime and orbiting planets with unknown gravitational pull using just a few bright lights to provide him with information and a lever that moved in only two directions. At that same point in history, PCB designers were creating the boards that helped to actually put people on the moon. And they did it using drafting tables, X-Acto knives, mechanical pencils, and stickers.

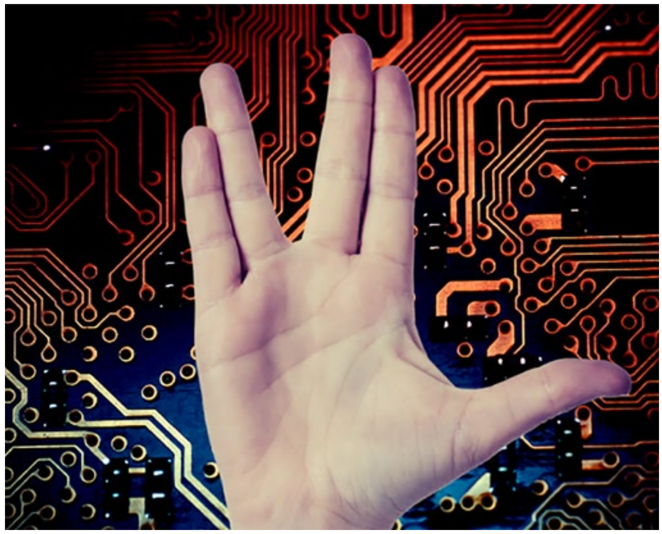
The Original Series

In the olden days, creating a PCB design was a two-person job—much like piloting the Enterprise. Without Chekhov to provide directions, Sulu would've been going in circles at warp speed. Without a trained electronics draftsman to create the schematic, PCB designers of that era would find themselves adrift on impulse power with shields at seven percent.

The process for drafting a board schematic in the pre-CAD era was like making schematics in construction. Schematics were built using pencils, a T-square, a triangle, a tilted table, and an eraser. Specialized electronics stencils were used to draw the schematic, ensur-

ing that components like capacitors and resistors would be consistent.

Once the schematic accuracy was verified, it was then given to the PCB designer. With schematic in hand, designers would grab their trusty component booklet and begin placing components—just like stickers—on a Mylar sheet with the aid of a light box. Even if boards of that era were comparatively much simpler than the ones we produce today, designing a PCB required a lot of painstaking effort. It was not unlike fighting the Gorn.



The Next Generation

As PCs—specifically UNIX workstations—became readily available tools for PCB designers in the 1980s, CAD tools changed everything. While Picard's Next Generation Enterprise had more lights, gizmos, and even a pet robot for their adventures, PCB designers began doing more with fewer tools. They shed their drafting tables and T-squares in favor of CAD software and a whole new set of skills.

CAD software evolved quickly and changed a lot over the course of *Star Trek: The Next Generation's* run on TV. At first, Data stood there repeating the word processing while he analyzed information, but by the time the gang was traveling through time to battle the Borg on the big screen, Data could process data quickly and silently. In that same time frame, PC capabilities grew by leaps and bounds—developing the ability to make the computations required by 3D CAD tools and access larger component libraries via the internet.

PCB designers could do more using CAD software, but they also had to know more and be able to work with a more complex decision tree during the design process.

The Expanded Universe

Today, keeping track of all the different *Star Trek* shows, movies, books, and podcasts is overwhelming to even the most rabid Trekkie. The same can be said for choosing the right CAD tool for your design. Do you pay for something with a larger feature set such as OrCAD or Altium or choose to rely on free or "simple" electronic design automation (EDA) tools?

We suggest sticking with the basics like they did in the original show. You don't want a complex matrix of bells and whistles when a lever that moves in two directions will do. And choosing a software with more functionality than you'll ever need can be confusing, like the new Picard series. Look for tools that will:

- Be easy to learn
- Have an intuitive user interface (UI)
- Possess features key to your design needs
- Include access to an expansive parts library
- Be in widespread use
- Generate Gerber files usable by most manufacturers
- Integrate smoothly with your manufacturing process

We believe this is the best way for designers on a continuing mission to improve quality, increase functionality, and fuel the innovative devices of tomorrow. **DESIGN007**

Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, click here.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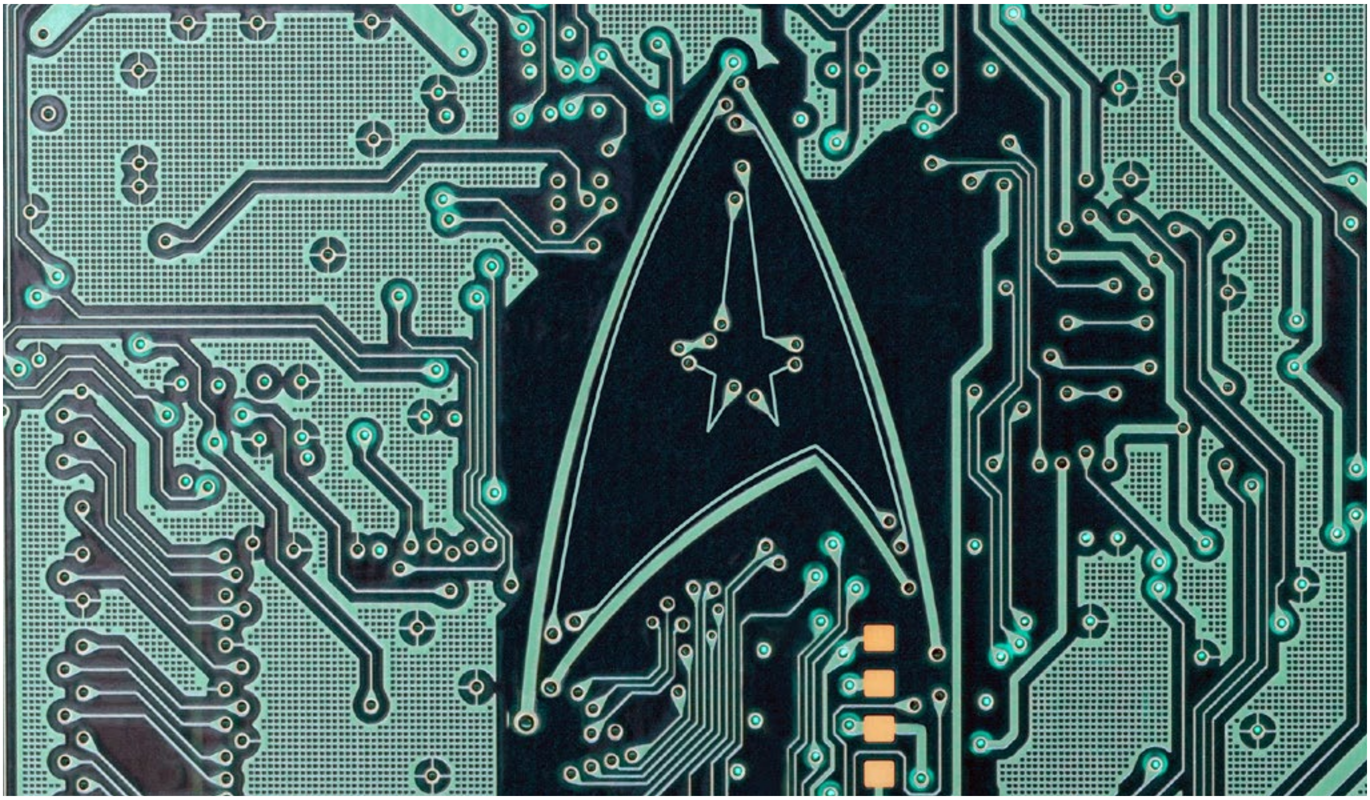


Star Trek: Laying a Path for Technology of Tomorrow, Today

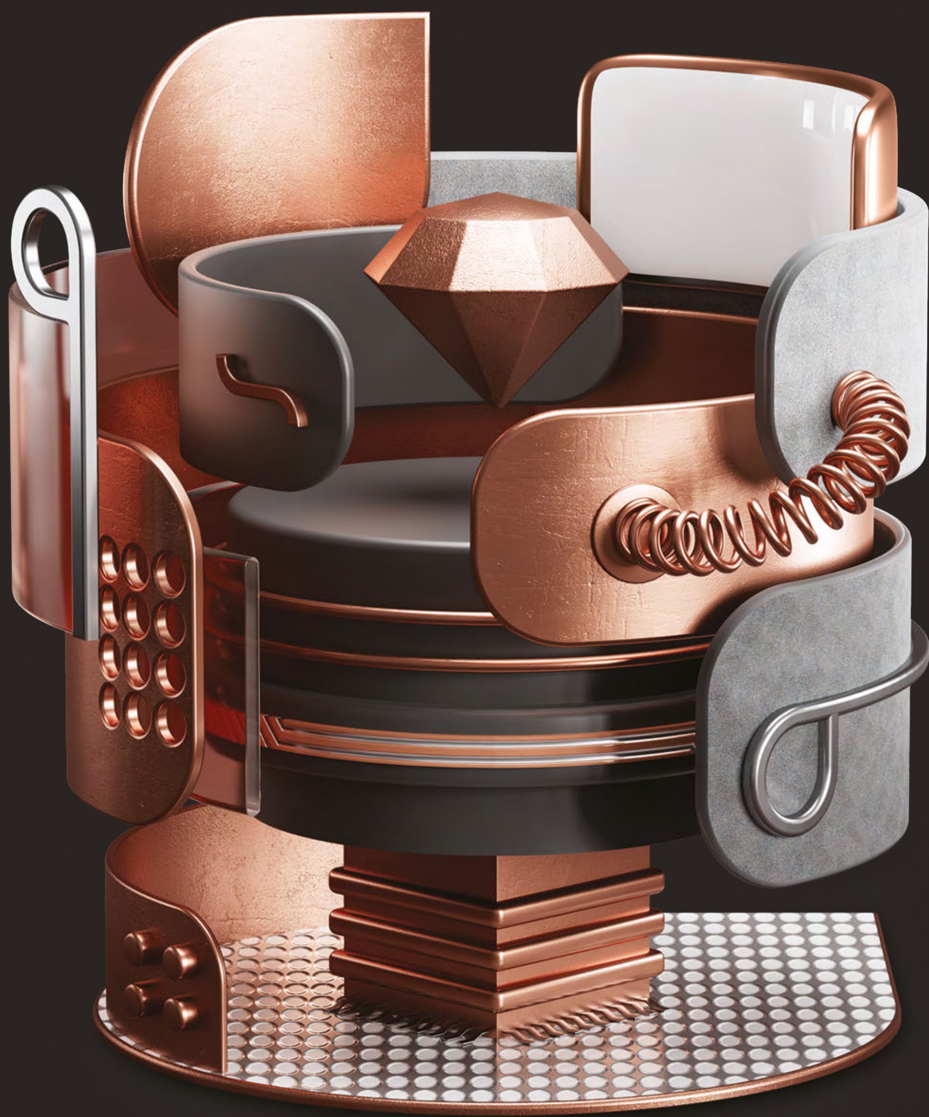
Feature Article by Alex Belelovsky
SIEMENS EDA

Tomorrow is Yesterday

In 1966, when *Star Trek* first aired, PCBs were in their infancy. A handful of components mounted to a double-sided board with 25-mil traces was on the leading edge of electronics. Since then, much of electronic innovation has been driven by PCB technology. Could the trends in PCB innovation have been predicted at that time? Perhaps through science fiction like *Star Trek* we can boldly explore our own final frontier.

Star Trek has always taken the universe it inhabits very seriously, always stretching our current understanding of technology by creating a world where we accept the extraordinary as possible. They have done this by taking our understanding of current technology and extending it to its logical and plausible extremes.

This methodology has amazingly predicted cellphones, voice-activated computers, and transparent aluminum, but can it be used within the PCB industry? The demand for more complex PCBs has resulted in new and enhanced design demands and production technologies, processes, and materials that not necessarily have gone hand-in-hand along the way. Did *Star Trek* work to predict this?



Mirror Mirror

Let's start with reviewing the main forces that have driven PCB technology in the recent decades—and most likely will keep driving it for years to come.

Miniaturization

Star Trek technology has always focused on miniaturization; the original series featured tiny cathode ray tubes on portable scanners. Over the run of the show, communicators shrank from hand-held devices to pins worn on your clothing.

Miniaturization has been so ubiquitous within our society that it has been reflected within the series reboots. In the Kelvin timeline (alternate reality), Hikaru Sulu, for example, carries a folding sword, a gadget that he likely keeps on hand in case of an impromptu polywater intoxication.

Since the early 2000s, every one of us has owned a handheld device that would outperform the most powerful supercomputer of the 1960s. Under the hood, smartphones hide multilayer, high-density boards with hundreds of components under severe physical size and weight restriction.

Since the early 2000s, every one of us has owned a handheld device that would outperform the most powerful supercomputer of the 1960s.

Computational Power

At the same time we see miniaturization of hand-held technology within the universe, we have also seen examples of the opposite happening—each iteration of the Enterprise is a little bigger, many of the ships larger. A good comparison might be looking at the size of the Doomsday machine in the original series to the Dyson Sphere in *Star Trek: The Next Generation.* The second is orders of magnitude larger than the first. When relaunching the series, there has always been some element of superpower present. Whether it is V'Ger in the *Star Trek: The Motion Picture,* or the Narada, Nero's ship from the 2009 movie, size, power, and complexity are always present.

In reality, autonomous cars, electric vehicles, medical electronic instruments, internet-of-things devices—all these and more require complex and powerfully interconnected electronics. Industry is moving toward a more collaborative manufacturing experience, with cloud-based DFM tools like PCBflow enabling and streamlining this collaboration, your fabrication partner's manufacturing constraints are instantly available to you.

The Trouble with Tribbles

Interesting enough, while these trends can look quite contradictory one to another, they result in the same trends in PCBs: high density. While there are many definitions for high-density interconnect (HDI) boards, they all agree that they contain fine traces, small spacings and laser vias.

On HDI boards, real-estate is expensive. It is advisable to use every 0.1 mil available to make fine trace spacing larger in order to increase the fabrication yield. Setting different target spacing values for different features with respect to their functionality can make all the difference.

Under no density constraints, it is quite common to route different traces using the same width. With HDI boards containing fine traces and tough spacing constraints, it is helpful if mission-critical traces are slightly wider when spacing allows. Even 0.1 mil can make a tangible difference in fabrication yield.

Perhaps surprisingly, these fine traces are produced in the same fashion as larger traces,

by way of chemical etching. While equipment, materials, and processes have been enhanced along the years, the etching process is inaccurate by its nature, leaving PCB fabricators in a continuing mission to increase its accuracy and its yield. The smaller the spacing between unexposed copper features on the board, the higher the chances that the fluid will flow non-uniformly, creating unwanted over-etching in places prone to this.

Most routing tools will ensure that traces make 135-degrees turns, but fine traces in dense areas may sometimes break on these turns, too. Thus, in case of thin lines in dense busses, you might consider making smooth turns using arcs or curves.

Every fabricator independently determines which places are prone for over-etching based on their experience. They may identify features as problematic such as a single pad in close vicinity of a long trace, two long traces that run in parallel, and separate or non-parallel traces that get too close to each other at a very small angle.

Return to Tomorrow

Are current HDI boards our industry's final frontier? No. Within our industry there is never a final frontier. We exist in an industry of efficiency and evolution. While great strides have been made in the HDI manufacturing, driven by miniaturization and computational power needs, we see additive and semi-additive processes arising to overcome limitations of HDI processes. However, these processes have not yet reached their maturity, while the miniaturization and computational power demands do not stop.

Are current HDI boards our industry's final frontier? No. Within our industry there is never a final frontier.

With more complex and denser board designs, your knowledge of fabrication becomes much more critical. Staying in touch with your fabricator is one of the best ways to prepare your design for optimal yields, and you don't need a fancy *Star Trek* communicator to do so. **DESIGN007**

Alex Belelovsky is software engineering manager at Siemens EDA.

High-Speed Serial Link PCB Design

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Serial communication has been used long before computers ever existed. The telegraph system using Morse code is one of the first digital modes of communication. All you need are two connections, which makes it simple and relatively robust. One wire is the signal and the other (dirt) ground. By interrupting the power with predefined patterns, information can be transferred over both short and long distances. The challenge is receiving the patterns correctly and quickly enough to be useful.

The simplest method of transferring data through the inputs or outputs (I/O) of ICs is to directly connect the data path from one IC to the next in parallel. But since most data consists of more than one bit of information the parallel data path is multiple bits wide. This is fine for signal routing between ICs on a multilayer PCB over short distances. For instance, DDR memory devices take advantage of the fast data transfer rates of the parallel bus. However, it has two inherent problems for high-speed data transfer over long distances. The first problem is that one I/O pin is required for each data bit. The second involves meeting timing requirements. Due to these two issues, parallel data is typically transformed to a serial data stream using serializer/deserializer (SERDES) modules (Figure 1) for high-speed communication links.

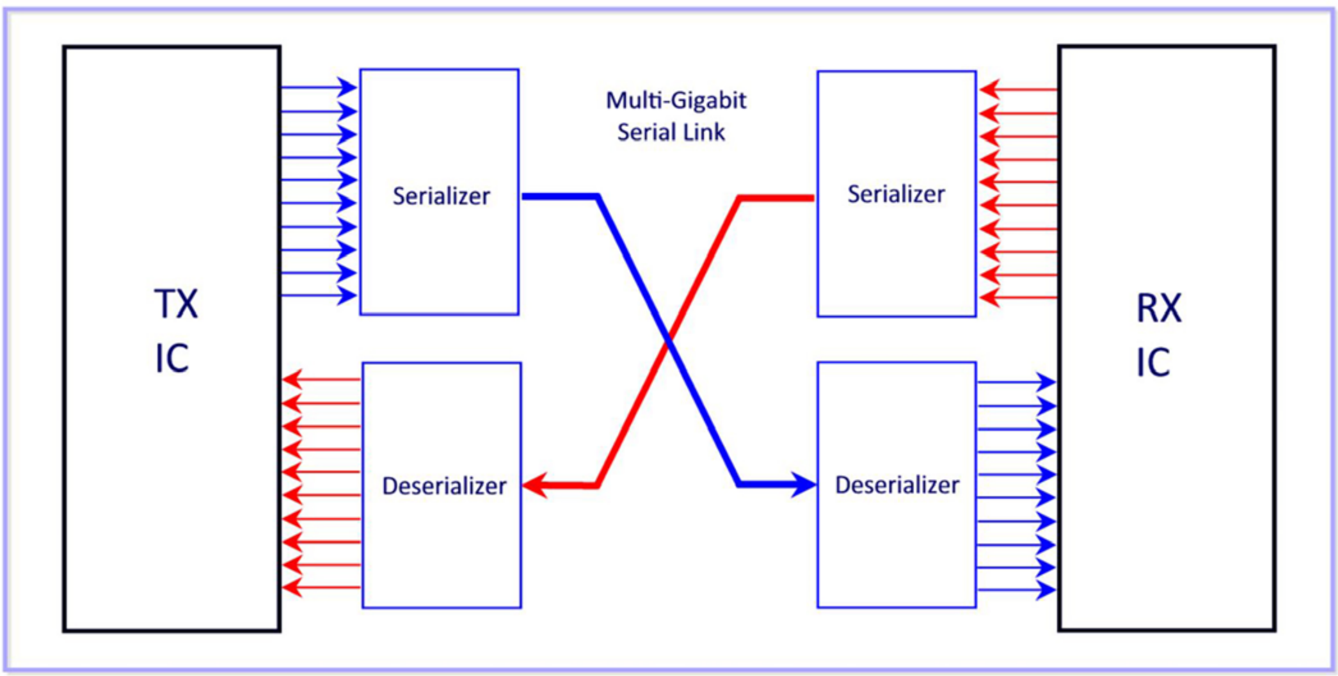


Figure 1: SERDES architecture.

Serial and parallel communications currently and historically co-exist and serve many requirements of intrasystem and intersystem data exchange. For instance, a parallel clock SERDES combo is normally used to serialize wide data-address-control parallel buses such as PCI. The choice of method is usually a tradeoff on factors such as speed, cost of materials, power consumption, and difficulty of physical implementation.

In principle, parallel communication is intrinsically faster than serial, because the speed of a parallel data link is equal to the number of symbols sent in parallel times the symbol rate of each individual path. Doubling the number of symbols sent at once doubles the data rate. For this reason, parallel communication is widely used in internal buses of integrated circuits and short distance IC-to-IC links. However, parallel communication is being replaced by serial communication in high-speed data links. These links include IC-to-IC communications on backplanes, computer networks, computer peripheral buses, long-haul communications, etc. The conventional reason to choose serial communications instead of parallel communications is cost.

High-speed SERDES devices are the dominant implementation of I/O interfaces at speeds of 2.5 Gbps and higher. Such devices are differentiated from a source-synchronous interface in that the receiver device contains a clock data recovery (CDR) circuit. This dynamically determines the optimal sampling point of the data signal based upon the transition edges of the signal. In other words, clock information is extracted directly from the data stream rather than relying on a separate clock. Also, signal integrity concerns frequently dictate that the data signal be equalized at the transmitter and/or receiver to counter the effects of the transmission channel and decode the signal properly.

Ten-bit transmission code was developed by IBM in the early 1980s. Called the 8b/10b code, the serializer maps each parallel data byte to a 10-bit code onto a serial pair. This code guarantees both multiple edge transitions every cycle as well as DC balance. It also provides a way to check for errors and send control information. Frequent edge transitions in the stream allow the receiver to synchronize the incoming data. DC balance facilitates driving AC-coupled loads, long cables, and optical modules. 8b/10b SERDES coding is well suited to serializing data such as cell or packet traffic across backplanes, cable, and fiber. Many standards such as ethernet, fiber channel, etc., use the popular 8b/10b coding at high data rates.

Implementing high-speed serial links can be challenging for the PCB designer. Any small discontinuity in the physical geometry along the transmission path can significantly degrade the signal. This degradation includes loss of amplitude, reduction of rise time, and increased jitter. As a result, one must be able to identify these discontinuities in the high-speed channel and mitigate their impact to improve the performance of the signal transmission.

A capacitor is typically placed in series with both differential signals to remove common mode voltage differences between ICs or different technologies. An “AC coupling capacitor” or “DC blocking capacitor” basically refers to the same thing. Any capacitor placed in series with the signal path tends to pass the high-frequency AC portions of the signal, while simultaneously blocking the low-frequency DC portions. These capacitors are essential to a variety of high-speed interfaces. And, as the next generation of designs target data rates of 56 Gbps and above, it becomes increasingly important to characterize channel transitions accurately to ensure a high confidence of success. As such, PCB designers need to take particular care routing serial interconnects.

It is always best to route critical signals on internal stripline layers. However, since the AC coupling capacitors are placed on the outer microstrip layer, routing on the outer layers becomes necessary to avoid discontinuities, layer transitions, and via stubs that create reflections. The most important parameter of the AC coupling capacitor is its relative geometry with respect to the substrate. The capacitors are placed in series with high-speed traces and, as such, the capacitor body becomes a section of the transmission line.

There are two approaches to placement and routing of the AC coupling capacitors:

1. To eliminate the excess parasitic capacitance associated with surface mount lands, a portion of the reference plane that is directly beneath the component can be removed. This allows the signal that traverses through the capacitor to reference a lower plane (further away) and reduces the parasitic capacitance, thereby minimizing the impedance mismatch (Figure 2).
2. A more elegant alternative is to use a smaller capacitor such as a 01005. The explicit assumption (above) is that capacitor land width exceeds the trace width and hence represents a short section of transmission line that requires a cutout to maintain impedance. However, a 200 µm trace can be used in conjunction with a 01005 package of 200 µm land width to avoid the impedance mismatch altogether. In this case, the cutout is not required (Figure 3). Note that the required wider trace will reduce the impedance, so a thicker dielectric will be necessary to control impedance.

There are two compelling arguments for the placement of AC coupling capacitors. The first

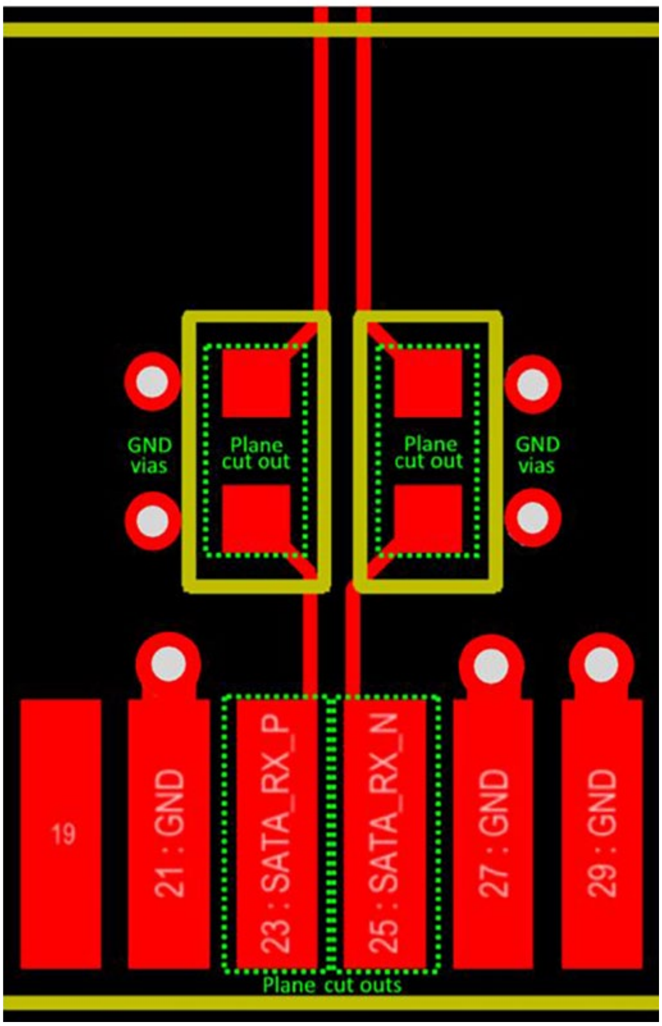


Figure 2: Plane cut-outs.

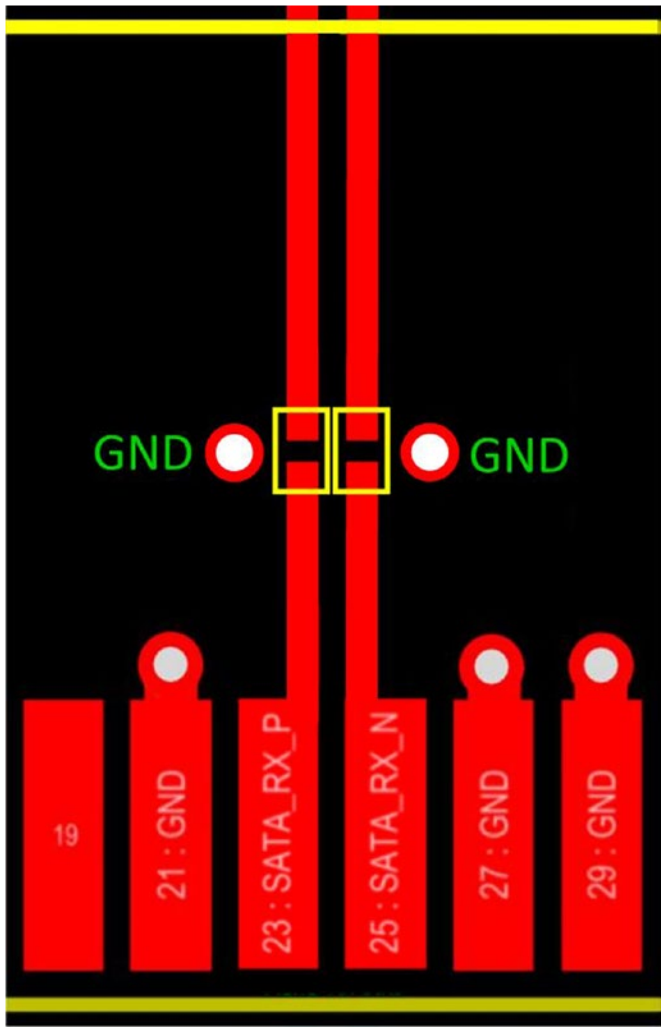


Figure 3: 200 µm trace with 01005 capacitors.

argument is to put the AC coupling capacitor close to the receiver and you'll be good, since all of the reflections will be smaller due to transmission line attenuation. This represents a time domain view of the world. The second argument is that for most passive interconnects, S-parameters are reciprocal (S21 = S12). Under this pretense, for a particular topology, as long as the distance from the endpoints to the AC coupling capacitor is the same, it does not matter if you place the capacitor at the receiver or driver, because the results will be identical. This represents a frequency domain view of the world. However, in practice it's slightly arbitrary. Often it's defined by a standard and the capacitors are specified on one end or the other end or occasionally on both ends. For instance, PCIe (PCI Express) specifies the AC coupling caps on the TX side, as there are methods it uses for detecting if a downstream device is connected that depends on that particular AC coupling configuration.

The other issue with routing serial links, on outer microstrip layers, is the solder mask coating. Having solder mask on microstrip traces will make them more unpredictable since it's difficult to control the thickness of coating on the top of traces and in the valley between them. So, if the solder mask is removed around the traces, it can improve the channel performance. However, there are a few down sides to this:

1. Depending on the substrate used, you might also find that humidity can enter the substrate surrounding the traces and may impact the impedance (solder mask is a very good water seal, so you will usually not see this effect with covered traces).

2. Also, if you are using ENIG plating, be careful with how thick the gold and nickel layers are, since you might end up with narrowband resonance. At approximately 2.7 GHz, the resonant behavior of the nickel component in ENIG increases insertion loss. This resonance is attributed to the ferromagnetic properties of the nickel layer. It is therefore wise to avoid using full body ENIG coating of microstrip traces at high frequencies. Consequently, solder mask over bare copper (SMOBC) processing should be considered for all high-speed designs. However, solder mask only impacts signal integrity above 12 Gbps.

Alternatively, to avoid the solder mask issue altogether, one could run differential serial links on the second layer of a dual build-up microstrip construction. This stabilizes the signal as it has a layer of prepreg over the traces. However, it will have impedance discontinuities due to the blind vias between layers 1 and 2 but this is practicable negligible.

When high-speed differential serial signals travel between boards, the destination location could have a different level on its ground. So, the transmitter and receiver could have different reference levels. A different ground level would cause the signal to appear to have a level shift that might make its level out of range for the receiver. AC coupling allows the receiver to change (bias) the signal reference levels to be compatible with the receiver's input levels. However, PCB designers must be able to identify any discontinuities in the high-speed channel and mitigate their impact to improve the performance of the signal transmission.

Key Points

- The simplest method of transferring data through the I/O of ICs is to directly connect the data path from one IC to the next in parallel.
- DDR memory devices take advantage of the fast data transfer rates of the parallel bus.
- A parallel clock SERDES combo is normally used to serialize wide data-address-control parallel buses such as PCI.
- Parallel communication is intrinsically faster than serial.

- High-speed SERDES devices are the dominant implementation of I/O interfaces at speed of 2.5 Gbps.
- Implementing high-speed serial links can be challenging for the PCB designer. Any small discontinuity in the physical geometry, along the transmission path, can significantly degrade the signal.
- A capacitor is typically placed in series with both differential signals to remove common mode voltage differences between ICs or different technologies.
- Any capacitor placed in series with the signal path tends to pass the high-frequency AC portions of the signal, while simultaneously blocking the low-frequency DC portions.
- Routing serial links on the outer microstrip layers becomes necessary to avoid discontinuities, layer transitions, and via stubs that create reflections.
- The most elegant solution to AC coupling is to use a smaller capacitor such as a 01005. A 200 µm trace can be used in conjunction with a 01005 package of 200 µm land width, to avoid the impedance mismatch.
- The AC coupling capacitors should be placed close to the receiver unless defined by a standard whereby they are specified on one end or the other end, or occasionally on both ends.
- Solder mask on microstrip traces will make them more unpredictable since it's difficult to control the thickness of coating on the top of traces and in the valley between them.
- If you are using ENIG plating, be careful with how thick the gold and nickel layers are, since you might end up with narrowband resonance.
- Solder mask only impacts on signal integrity above 12 Gbps. **DESIGN007**

Resources

For more on this topic:

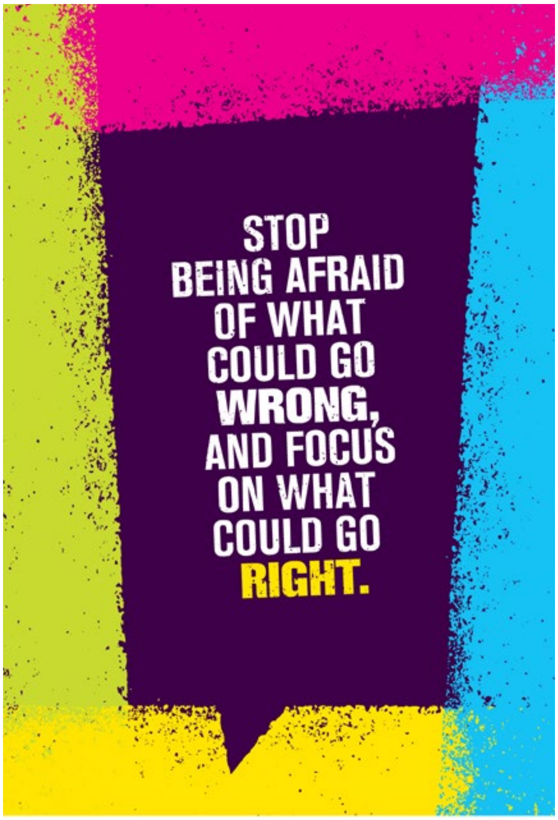
1. Beyond Design: AC/DC is Not Just a Rock Band, by Barry Olney, Design007 Magazine, April 2018.
2. Surface Finishes for High-Speed PCBs, by Barry Olney, The PCB Design Magazine, June 2014.
3. High speed serial link (SERDES), Introduction, Architectures and applications, by Abdallah Ashry, academia.edu.
4. Serializer and Deserializer (SerDes) for High-Speed Serial, by Dianyong Chen, et al.
5. High speed interconnect optimization, by Mallikarjun Vasa, et al.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, click here.

Managing Risk in PCB Design

Elementary, Mr. Watson

by John Watson, ALTIUM



I recently attended a risk analysis meeting that focused on the question, "What can go wrong in a system design?" They slowly worked their way around to me. As the senior PCB engineer, my first thought was, "This is a loaded question." My answer, though, was short and sweet: "Anything and everything."

That is so true, though; I have seen some crazy things during my 40-year career. One of the weirdest things I saw in a PCB design many years ago was that underneath the PCB solder mask there looked to be a mosquito—like a fossil of some prehistoric creature right there in the middle of my board. I couldn't believe it. I was expecting the board fabricator to come back and say, "You should have included a note on the fabrication drawing saying, 'Please make sure no mosquitos are implanted under the solder mask.'"

Not much was accomplished in that meeting because, you see, the starting point was all wrong. To begin a conversation based on the "what ifs" of what could go wrong is both an impossible question to answer and an exercise in futility. It is unquestionably the incorrect way to handle risk management, especially in the PCB design process.

PCB Design is a High-Risk Process

PCB design is like bungee jumping. With the complexity of a PCB design, the intricate details, and various steps, it's rather easy to make mistakes. Those mistakes, many times, do not show up until it's too late and the board has gone off to fabrication and assembly. By the way, a good rule is to not use your assembly house as your quality control team for PCB designs.

Furthermore, you are not in control of the complete process since it involves third-party vendors outside your company. Managing the risk that is not under your control is even more difficult. Before taking a deep dive into the risk management area, we need to understand that the PCB design is a by-product of your process and design data. If either one of those is incorrect, your PCB will be built wrong.

Managing this risk is vital if you intend to keep your job as a PCB designer. So, what is the correct process to identify the risk and put in place the required solutions before they get

into your design? As we have already seen, good risk management does not occur from the top-down based on the "what-ifs" but rather from the ground up, examining and controlling your process.

The management of any risk must start early and often, and look at the process that results in that design. If you only conduct risk management processes on the finished goods, you may find yourself a day late and a dollar short.

Also, no matter what measures you put in place, you cannot entirely remove all risks from your PCB design. But, with some simple steps, you can reduce the probability of problems.

Steps of Risk Management

Identify the Risk in your Process

The first step in managing the risk in your PCB is to identify the weakest links in the process. Fortunately, a PCB design process is linear and in a controlled environment, which means that you begin the process with a known data set, which for us is the component library. I have said it before, if you do not manage your library, your designs are doomed to fail. Then the process continues with periodic checks made at crucial points to verify that everything is still on track. These are gate-keeping items, and the design should not proceed until they pass successfully.

With that said, the first step in your risk management plan is to determine the locations in your PCB process of the weakest area and where there are no checks to catch problems. For example, many years ago, there were no automated checks done on the components in your library. Everything got manually reviewed, meaning they were prone to mistakes. That introduced a huge risk into your PCB with either completely unchecked or partially checked components.

Evaluation of Risks

Once you have identified the weak areas in your design process, you must identify those areas with parameters used to devise a control strategy. In that way, you can quickly determine the likelihood of a risk occurring and what actions need to happen—taking our example earlier with unchecked components. The possibility of problems arising at that point of the design is relatively high. That is where you must focus on the next step of controlling the risk.

Controlling the Risks

Here is where the risk management plan begins to develop. Once you have identified and evaluated the risks, you now know where the risk is occurring, and you have the parameters by which you will determine the severity of the risk. Now we can start to develop the plan to manage the risk.

Keep in mind that improvements in your PCB design process also mean improvements in your PCB quality.

We are continuing with our example of unchecked components. Such a solution is to set a process in place to QC all new components. Many PCB design software tools now check the components, which would be the first step, then conduct additional visual checks of each part of the component.

Review the Risk Controls

Risk management is not a process that is set in stone. Instead, it is something that is constantly reviewed and polished. Especially when problems occur, as we will see coming up, we must review the risk controls in place and determine how we improve on them. That means there is no finish line to risk management. Instead, it is something that is much more fluid and changing. I guess the best rule is to be flexible. It will go a long way to improving your process.

When Things Go Wrong, Identify the Root Cause and Enact a Solution

As mentioned before, you cannot remove all risks from any process, so what do you do when a problem raises its ugly head? It is not enough to identify the "obvious" problem; what you see is only the result of the cause. You need to dig deeper and determine the root cause. You can quickly identify the root cause of an issue by using the "five whys." That is a technique that digs deep into a problem by asking "why?" You must do that at least five times to get to the root cause of an issue.

For example:

I come out to my car, and I find my car has a dead battery.

1. I have a dead battery. Why?
2. The alternator is not charging the battery. Why?
3. Alternator belt is loose and frayed. Why?
4. The belt has reached its end of life. Why?
5. Did not replace the belt during the required maintenance. This is the root cause.

If you did not go through this process, you might be quick to replace the dead battery and never fix the real issue and root cause of the problem. You might be shocked that what got identified as a problem was not even close to the root cause. It's essential to find the root causes. Otherwise, you are only looking at the effect. Ultimately, nothing gets solved. The solutions for the problem all flow directly from that root cause.

My last point is that with a complex process like PCB design, risk management is essential. We've all heard this idiom: The definition of insanity is doing the same thing and expecting different results. You may see the problems but never learn how to tackle them. Don't keep doing the same old things that don't work. Get control of your design process and manage the risk. DESIGN007

John Watson, CID, is customer success manager for Altium. To read past columns or contact Watson, click here.

Intelligent Antenna Passes the Test

An intelligent antenna developed by researchers at Waterloo Engineering has been successfully tested, a major milestone in a multi-year, multi-million-dollar project.

"This modular, intelligent technology platform provides a cost-effective solution for a wide range of applications—from fixed to mobility satellite broadband services, and for the rapidly emerging millimeter-wave 5G cellular services," said Safieddin (Ali) Safavi-Naeini, director of the Centre for Intelligent Antenna and Radio Systems (CIARS) at Waterloo.

Operating on the Ka-band, the low-cost technology was used in tests to stream video, surf the Internet, perform speed tests and conduct an uninterrupted video conference over Webex.

Safavi-Naeini has been working on intelligent antenna systems for satellite-based internet connectivity for almost two and a half decades, motivated by their potential to deliver broadband service via satellite to moving vehicles and bridge the digital divide by extending the reach of broadband Internet to vast areas of the world that lack access.

"Measured over-the-air results have demonstrated the high performance of the compact, scalable antenna modules and validated our modular technology architecture for larger panels," he said.

Researchers will now continue testing over several different satellites to confirm interoperability of the new antenna and radio system.

(Source: University of Waterloo)

Some 'Exotic' PCB Processes Could Become Commonplace

Lightning Speed Laminates

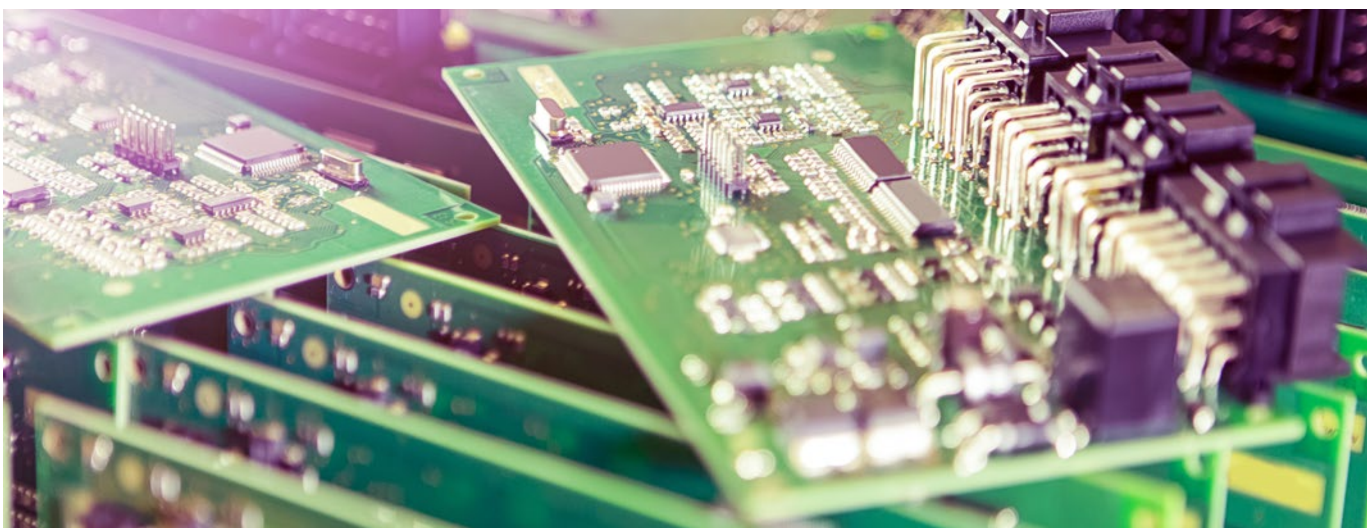
by John Coonrod, ROGERS CORPORATION

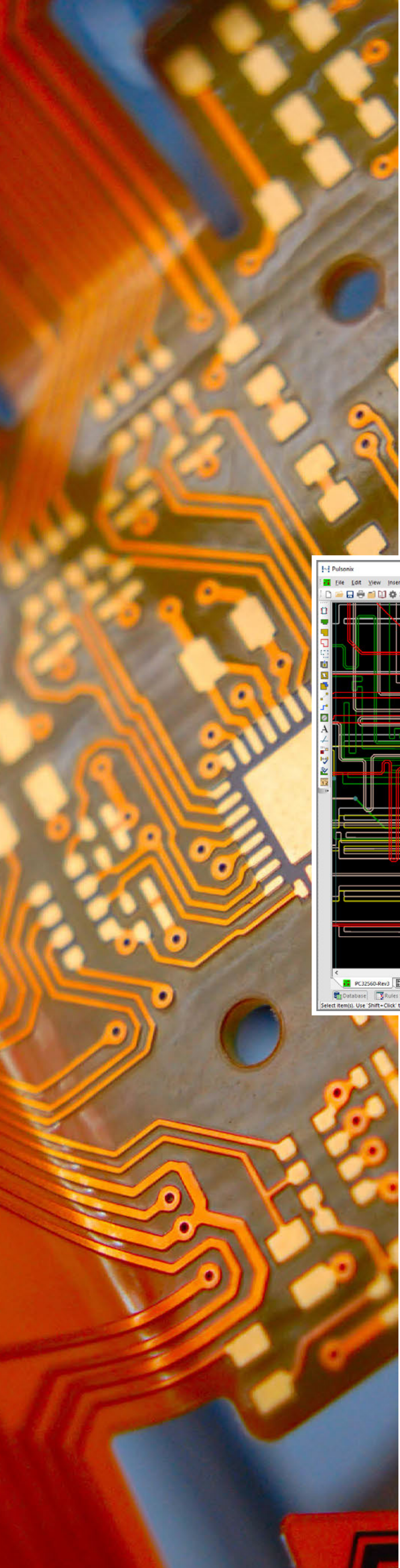
Technology is advancing quickly and over the years the PCB industry has advanced its processing and capabilities extensively as well. However, due to technology demands, it is likely that some of the processes for PCB fabrication that were previously considered exotic may soon be considered commonplace. Of course, that prediction depends on many issues. Due to the nature of new and evolving applications, the PCB industry will likely need to make more advances in some of its processing.

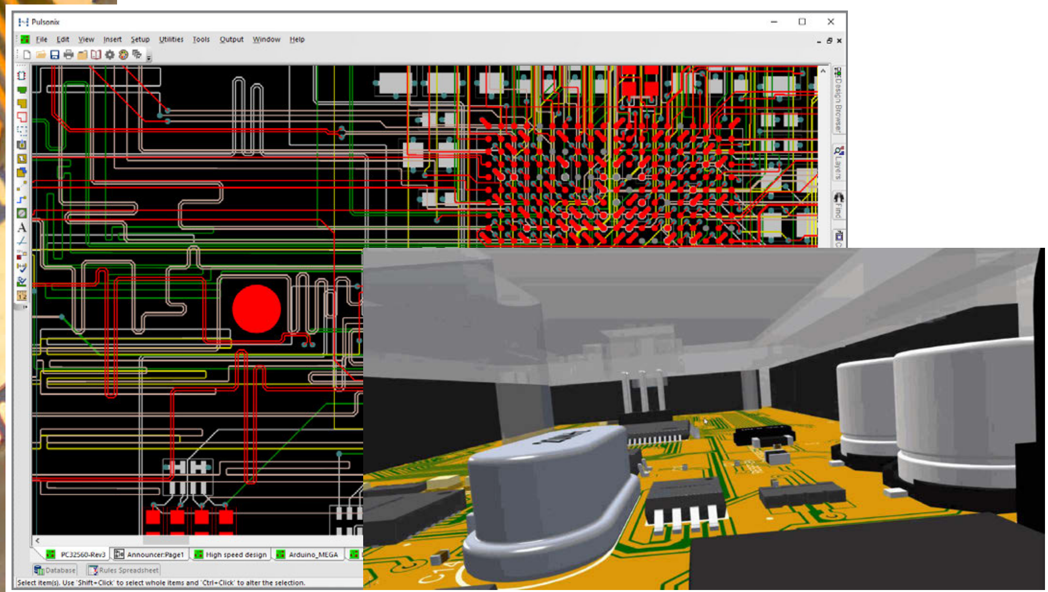
Those PCB fabricators who support 77 GHz automotive radar applications are probably very aware of the stringent requirements for these very high frequency applications. Generally, applications at higher frequencies will have more sensitivity to several PCB processes and their normal variations. One simple example is circuit etching quality, and for many mmWave applications, the conductor widths are commonly required to be held to tighter tolerances. The trapezoidal shape of a signal conductor is often specified to be within a certain range and even the roughness of conductor sidewalls have shown to cause RF differences at 77 GHz. Copper plating thickness variation can also be very problematic; having tight control of this process is important for very high frequency applications.

There are several new applications using PCB technology above 77 GHz which require processing capabilities that exceed the current PCB technology. A lot of research work is being done, for example, around 140 GHz for a particular application. The conductor width tolerance needs to be ±1 micron (0.04 mil), conductor thickness needs to be very thin (2 micron), and the thickness variation needs to be at ±0.5 micron. There are some other specifications which are also extremely difficult, or maybe impossible for current PCB technology, such as very tight location tolerances between circuit features and microvias and layer-to-layer alignment.

One of the 140 GHz applications I read about in a white paper on IEEE.org used a combina-







tion of PCB technology and semiconductor technology. The main board was made with PCB technology and that circuit board had 35 GHz for the highest operating frequency. That circuit board is no problem for our current PCB fabricators to meet the requirements. However, mounted on the main board was a small glass circuit made with semiconductor technology and that circuit had castellated vias at the edges, which were used to solder-connect to the main board. The 35 GHz signal on the PCB would transition through the castellated vias onto the glass circuit and it would go through a 4x frequency multiplier to get the signal up to ~140 GHz.

After that, the 140 GHz signal would be processed as necessary on the glass circuit. That is a very interesting way to deal with a 140 GHz application, but I would question the capability of high-volume manufacturing as well as cost concerns. If PCB technology can be used to generate circuit features with extreme precision, the high frequency circuit materials that we currently offer can support this technology and have benefits over the glass semiconductor technology.

One PCB technology that has been around for many years is laser-defined conductors. Some of the recent laser technologies can generate high precision circuit geometry. There are limits to these processes currently, but over time, and if the PCB industry develops this technology for high-volume, this could be a process used for the future millimeter-wave PCB circuitry.

Another PCB fabrication process, which may be beneficial for the industry to exert some effort in advancing, is fusion bonding technology. Fusion bonding has been around for many years, but typically not done in high volume manufacturing. There are many things to overcome to make this technology robust for high volume manufacturing while still maintaining the exceptional electrical properties it can offer.

Fusion bonding uses very controlled lamination equipment and processes to basically melt a thermoplastic material, which acts as a bonding material for a multilayer circuit. It will not surprise those engineers who have investigated different high-frequency materials that there is one type of material that stands out for the best electrical performance, especially for very high frequency: PTFE-based material. To laminate a multilayer that uses a PTFE-based bonding material, a fusion bonding process must be used.

A few years ago, Rogers Corporation brought to market a set of PTFE-based materials specifically formulated to meet the electrical needs of very high-speed digital (56 Gbps, 112 Gbps, etc.) applications. The material is Rogers XtremeSpeed RO1200 family of products, and several independent studies have shown this material set can achieve the best electrical performance for very high-speed digital applications.

However, to get the optimum benefit of this material set, the lamination of the multilayer circuit using this material will need to use the XtremeSpeed RO1200 bondply and a fusion bonding process. (As a quick side note, we have achieved very good high-speed digital results when using the XtremeSpeed RO1200 core with SpeedWave 300P prepreg. SpeedWave 300P prepreg does not need fusion bonding and it will have lamination process parameters more common for high-volume PCB fabrication.) A pure package PCB using XtremeSpeed RO1200 core with XtremeSpeed RO1200 Bondply has the best electrical performance for the most demanding high-speed digital applications. These materials can support the upcoming advanced high-speed digital requirements of the future. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

PCB007 Highlights

Arlon President Discusses Acquisition by EMC ▶

Arlon President Brad Foster updates Nolan Johnson on EMC's acquisition of Arlon in December 2020. Foster shares the basic structure of the agreement, the long-term stability built into the merger, and outlines how this brings EMC, Arlon, and Technica together as a team. Foster also hints at what we can expect to see from Arlon and EMC in the coming months.

Testing Todd: A Point of Order—Do Not Just Rearrange the Pencils! ▶

In our concentration on continuous improvement, we should look into the order of things. Efficiency comes from streamlining processes, effective training, and the ability to monitor success through KPIs and feedback on deliverables.

The Right Approach: Leadership 101—The Law of Influence ▶

Good leadership always makes a difference; unfortunately, so does bad leadership. This leadership truth continues as we will be talking about the second of the 21 Irrefutable Laws of Leadership, The Law of Influence.

Benchmarking Your Process Engineering ▶

In this discussion with the I-Connect007 editorial team, Mark Thompson shares what's important from a process engineer's point of view, and how to stay on top of evaluating and benchmarking your manufacturing process, along with insights from his role as a designer.

Joe D'Ambrisi Discusses MacDermid Alpha's Acquisition of HK Wentworth ▶

Element Solutions' Executive Vice President Joe D'Ambrisi speaks with Nolan Johnson about MacDermid Alpha's recent acquisition of HK Wentworth. Joe shares some details on the transaction and outlines the expected benefits that come from bringing these two companies together.

The PCB Norsemen: Don't Forget AABUS ▶

The most important thing is to know a standard and how to use it. Here is all you need to know about AABUS, what it means, how to handle it, and basically a list of issues that needs AABUS.

Catching Up With Gardien's Niraj Patel ▶

Dan Beaulieu says he has always been fascinated by Gardien, especially two particular services they offer. First, they embed their team into a facility and actually take over as the PCB company's expert test center; second, they have a universal quality system to track problems and solutions from all over the world and then keep them in a universal database that can be shared by everyone. Dan recently reached out to Niraj Patel, Gardien's vice president in charge of North America.

Lenthor Engineering Adds ESI's GEODE CO2 Microvia Drilling System ▶

Lenthor Engineering, Inc., a California-based designer, manufacturer and assembler of flex and rigid-flex printed circuit boards, has purchased ESI's Geode CO2 microvia drilling system including the optional automated loading and unloading stations.

PCB Engineering on the Move

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

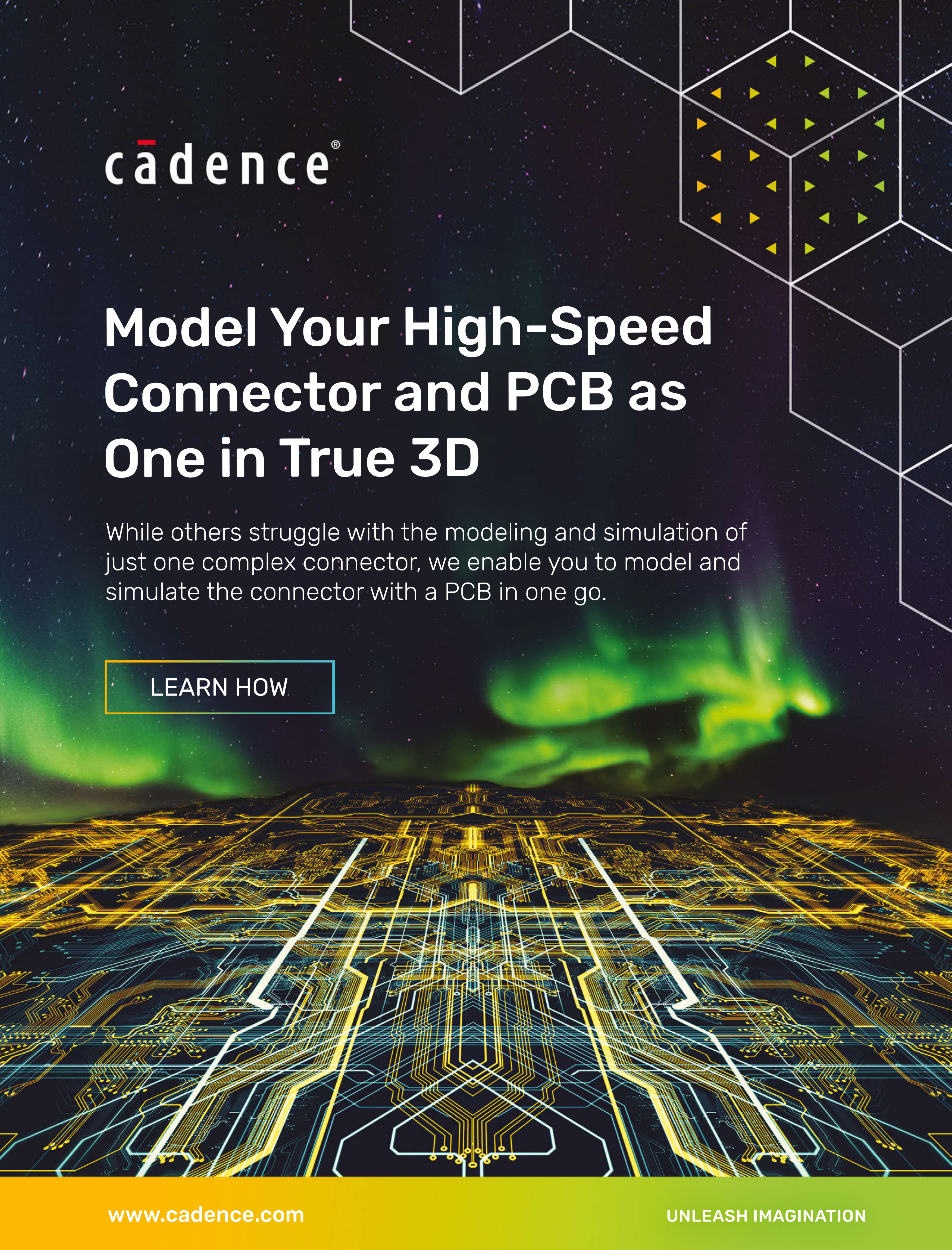
Introduction

In this month's column, I examine the PCB engineering job outlook and evaluate the career moves we are making. Next, PCEA Chairman Stephen Chavez shares some important attributes for personal development that will keep our edges sharp. Finally, I provide a growing list of industry events for 2021.

PCEA Updates

The pandemic came upon us like a supersonic jet—unseen and unheard as it passed over and through us. It compressed the atmosphere of our lives, our industry, and our jobs. As it appears to be moving on with the help of remote working, masking, social distancing, and vaccination, the industry is moving to positively decompress. NPI programs are revving up once again and causing sonic shock waves of hiring activity and job movement. Were you one who was furloughed, laid off, or had your hours cut back due to the effects of the pandemic? Boom! It's time to become an industry shock wave and clap back.

Check out the PCB industry hiring pages. There are pulses of hiring activity here in the Pacific Northwest—and most likely in your area as well. One PCB designer I know moved to a company that is staffing up for new projects, which left a void in his company. I am happy to have recently been given the opportunity to fill his position. But my movement left a void in the company I left, which is now trying to recruit another designer to fill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my place. Will they hire a designer who was previously laid off? Will another designer depart his or her job to fill it? Design resource movement will go on and on and hopefully that is a good thing if we all can learn from it.

So, what did we learn from 2020?

Regardless of the five Ws—who, what, when, where, and why—our present state of being is subject to unforeseen circumstances. We've seen that a supersonically growing economy can be put on hold by the smallest of organisms—a virus in this case. We've seen that our strengths can become weaknesses if not paired with the diverse strengths of others. We've seen that no one is an island. We cannot exist alone. We're in it together. Hopefully, we've seen that we need a healthy industry ecosystem full of workers—moving about—who are healthy in mind and spirit.

What must we do as we move forward?

> **We've seen that our strengths can become weaknesses if not paired with the diverse strengths of others.**

Germinate

Write down your ideas, visions, and goals. These are concept seeds which, upon sprouting, will help you to consider options to move positively within your organization. They can help you to become a positive shock wave and foster positive movement within or even without if the culture or atmosphere becomes too compressed.

Feed

Find your strengths and feed them. Upon starting my new position at a new company, I was delighted to receive a copy of a book by Don Clifton, *Discover Your Clifton Strengths.* This positive surprise let me know that the leadership of this engineering group is interested in helping me to understand my strengths and match them with the strengths of others in our engineering group.

Grow

We grow by pushing away the compost of our surroundings. We must push toward the light. As PCB engineering professionals, we must reach for technology and skill set nutrients which are easily found within the pages of this publication and the upcoming events sponsored by the PCEA and many other electronics industry organizations.

Transplant

Are you new to the PCB engineering industry? Maybe you consider yourself a seedling. You will need to learn all you can in your present position and then eventually transplant to avoid becoming root bound. Again, this may happen inside or outside your company, but it must happen. Look to your organization's management as your gardener. For the organization to benefit, you must grow. Are you an old timer in this industry? Your management team should consider you a valuable, aged, majestic oak. Most likely you have already been transplanted many times before and are thriving because of it. You provide shade and seeds for future ideas which can be planted anew. You make it easy for them to answer the most profound PCB engineering staffing question: "When is the best time to plant a tree?" Answer: "Thirty years ago."

Message from the Chairman

by Stephen Chavez, MIT, CID+

My message this month is short and simple. When it comes to printed circuit engineering, there is so much more to it than simply connecting the dots. It involves knowing how to design a PCB correctly, successfully collaborating with others, effectively communicating with both internal team members and your suppliers, and mastering your CAD system. These are all major attributes of most successful printed circuit engineers.

Stephen Chavez

As companies and engineering teams continue to push the envelope with their designs, the use of their CAD systems, and their ability to effectively work together in bringing their respective products to market on schedule and under budget, it forces many of us to constantly evolve and to continue our professional development. It's extremely competitive out there. Even as industry veterans with decades of experience and education, we must constantly keep evolving, learning to stay in shape, and be competitive so we don't get left behind or, worse yet, become obsolete. That's why PCEA is a great industry association to get involved with.

"Collaborate, Educate, and Inspire" is the core mission of PCEA. We share the latest industry information, technologies, educational content, and industry best practices. Building long term relationships both professionally and personally, as well as mentorships, are also topics one will find within the PCEA collective. A good example of these topics in motion was our most recent event with our Orange County (California) PCEA chapter. Scott McCurdy and his leadership team brought together approximately 100 attendees to address "Designing for RF—Tips and Tricks from the PCB Pros,"[1] presented by EMA, one of our (PCEA) sponsors. Kudos to Scott and his leadership team for putting on another successful event. I also want to thank EMA for bringing excellent industry content to the table, and for everyone who attended to add to their respective bags of magic. The collaboration between PCEA and EMA was another home run.

With so many industry webinars; Zoom, GoTo, and Teams meetings; and the flood of "free" online content out there now, we are bombarded. It's been "information overload" for quite a while now. It's hard to find the time to attend these industry events, and to decide which content is worth giving up an hour or more of your time for an online presentation, YouTube video, or podcast. But you can rest assured that if PCEA is putting on an event, or collaborating with another industry association, we are bringing you the best and most relevant industry content.

We've been on lockdown for over a year, but we are slowing coming out of it. I cannot wait to get back to attending live, in-person industry conferences. I'm sure most of you feel the same. Like always, we adapt to the times and the evolution of the industry as this new way of collaborating virtually, but there is no experience quite like attending an actual industry conference. I can't wait to see you all in person at the next industry event.

Our partnerships with industry sponsors allow us to present even more outstanding educational content when it comes to printed circuit engineering.

Over these next few months, we will be rolling out quite a bit more educational content as we integrate and collaborate with our sponsors. Our partnerships with industry sponsors allow us to present even more outstanding educational content when it comes to printed circuit engineering. I highly recommend you get involved with and join the PCEA collective, if you have not already. When you join and participate, your percentage of long-term professional development increases significantly.

I continue to wish everyone and their families health and safety. Best of success to all as 2021 continues to unfold.

Warmest regards,

—Steph

Next Month

Next month is hopeful and wide open for coverage of a potpourri of PCEA activities. Tune in to this column for the latest events and ideas.

Upcoming Events

Below is our list of upcoming events. Hope to see you at any of these.

- **Zuken Innovation World 2021 (Digital Edition)**
  August 4-5, 2021
- **DesignCon 2021**
  August 16-18, 2021
  San Jose, California
- **PCB West 2021**
  October 5–8, 2021
  Santa Clara, California
- **SMTA International 2021**
  Nov. 1–4, 2021
  Minneapolis, Minnesota
- **PCB Carolina 2021**
  Nov. 10, 2021
  Raleigh, North Carolina
- **productronica**
  Nov. 16–19, 2021
  Munich, Germany

Spread the word. If you have a significant electronics industry event that you would like to announce, please send details to kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Refer to our column and the PCEA website to stay up to date with the up-and-coming industry events: pce-a.org.

Conclusion

Sometimes it's just way too easy to describe our work in metaphor. This month, we covered PCB engineering career movement by drawing parallels to everything from sonic booms to Gardening 101. Whether we use metaphors or cold, hard numbers and statistics—as our PCEA Chairman Steph Chavez mentions—the goal of the PCEA is to collaborate, educate, and inspire. We want you to value yourself along with those you work with and work for. We hope we are reaching you.

See you next month or sooner! **DESIGN007**

References

1. To read a review of this webinar, click here.

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.


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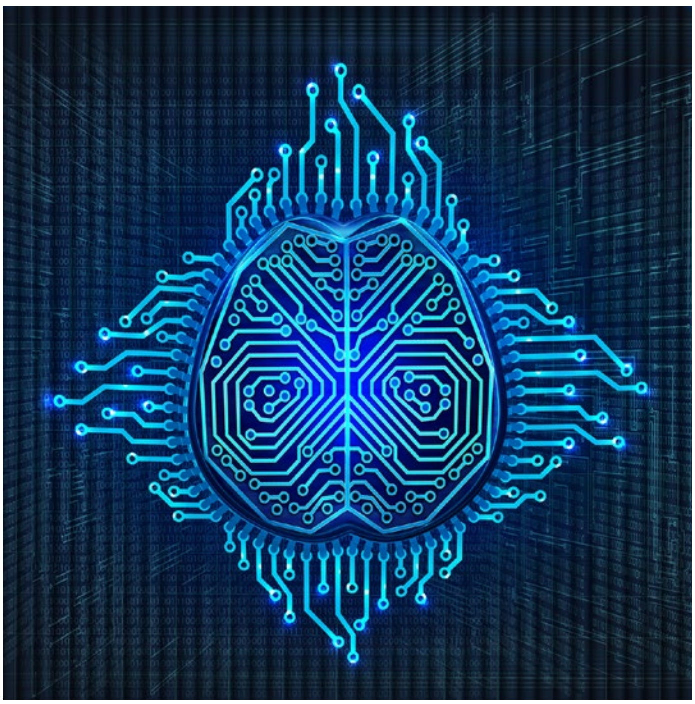
A Review of Additive Electronics

PCB Talk

by Tara Dunn, AVERATEK

Additive electronics, particularly as it pertains to PCB fabrication processes, is garnering a lot of attention. The ability to form much tighter feature sizes than typically available from subtractive etch PCB fabrication processes, along with significant RF benefits, is opening new possibilities for PCB designers as they work to navigate the increasingly complex balance between functionality, size, and complexity. As with any new technology, there is a learning curve for PCB designs. This is the second in a series of columns intended to shed light on the experience these early adopters have gained. Here, I speak with Tomas Chester, founder and hardware designer for Chester Electronic Design.



Tara Dunn: Tomas, you are a well-known designer and instructor in the industry, but for those who have not had the opportunity to meet you, could you please start with a quick introduction?

Tomas Chester: Sure. I am a hardware design engineer from Ontario, Canada. In 2017, I founded my own contracting and consulting firm, Chester Electronic Design. Since then, I have worked on all manner of boards from IMS to semi-flex. In 2020, I started the Ontario Canada PCEA Chapter, and in 2021, I joined the PCEA Executive Board. I am also a full-time Altium instructor for their Essentials and Advanced courses.

Dunn: That is an impressive resume. I am positive that founding your own contracting and consulting firm requires you to have knowledge in many different types of technology. One thing you and I have talked about quite a bit is the potential benefits of using 25-micron trace and space or below in PCB design. What were some of your initial thoughts? What caught your eye?

Chester: My initial thought jumped to the possible use cases in those ultra-small design

Tomas Chester

cases. I can see a lot of uses for technology like this in the medical space or even in the wearable devices market. Being able to have such small traces is going to enable not only smaller designs, but higher utilization of existing real estate, which will lead to the reduction of raw materials required to build a design.

Dunn: You had a few questions early in our discussions that I think are going to be common questions among PCB designers.

Chester: What trace-to-trace gap distance is possible?

Dunn: With the right photolithography set-up as small as 12.5 microns has been run. Most fabricators can do 20 to 25 microns.

Chester: As this is an additive process, how tall of a trace can you get? Can you control this height?

Dunn: Currently, for a 25-micron (.001") line, a 20 to 25 micron (.0008" to .001") thick line is standard with 50 microns (.002") possible but not tested. On a 50-micron line, a 50-micron thickness can be done.

Chester: How tight is the line-width control?

Dunn: This is very tight, typically ±1 micron (±.000039").

Chester: Do you need to use a special solder mask when using a very fine pitch semi-additive design process?

Dunn: No. Typically, the design will end up with an LDI imageable mask, but that is very common now. Consideration needs to be given to mask-defined pads over copper defined to keep the adjacent traces covered.

Chester: Where in the design fabrication process does this fit?

Dunn: The semi-additive process is completed early in the fabrication process. To oversimplify, where traditional subtractive etch processes start with a copper-clad laminate panel and etches away the copper that is not required, the semi-additive approach begins with the base dielectric and adds copper to the panel in only selected areas.

Chester: Can you mechanically drill with SAP, or do you need to use a special drilling process?

Dunn: Both mechanical drill and laser drill can be used with semi-additive processes. We are just scratching the surface on how best to apply these new fabrication capabilities to PCB design. There are obvious benefits to overall size and weight. There is also the potential to reduce layer count, reduce lamination cycles, and reduce the number of microvia layers needed, which all increase yield and overall reliability. What aspect of these new PCB fabrication capabilities is most valuable to you?

Chester: I think all designers are going to be excited with the ability to access some of these benefits. For me personally I am excited about the ability to breakout of the µBGA part without needing to do other HDI design strategies.

> I think all designers are going to be excited with the ability to access some of these benefits.

Dunn: You are currently working on a project that involves redesigning an Altium reference design, applying 25-micron trace/space where it makes sense. Can you tell us about the project?

Chester: To get a better understanding of some of the requirements and difficulties a designer would need to design an SAP product, I am using an existing Altium DDR4 SODIMM design to reimagine it utilizing SAP. This is resulting in some promising improvements with respect to layer reduction and it also has reduced the overall complexity of designing a DDR4 fly-by architecture. As with any engineering process, there are some assumptions that have been made with respect to the design as we are still in the early days of SAP, so this is intended as a learning and educational piece with an understanding that it may not be functional. However, as I said, it is more about the experience and getting that key information on how to implement SAP into a design and what improvements come out of it. The key in this situation is having an existing design that we can refer to and compare the changes once we complete the design.

Dunn: I am looking forward to those results. Working with something new can be exciting and just a little intimidating. In navigating the learning curve, do you see any challenges for designing with this new technology in mind?

Chester: I think that there are some challenges that will need to be overcome. Due to the changes in trace size and with respect to how new this process is, the impedance and the field theory around using this in a design is still being developed. The SAP process means we are shifting away from planar coupling of traces and starting to deal with broadside coupling and the requirements for co-planar wave guides. Currently there is no proper way to calculate what this is going to do at such a small scale, which could cause all sorts of design and signal integrity issues.

Dunn: Tomas, as we wrap up, what advice would you give to PCB designers who are just hearing about the opportunity to work with fabricators that can now offer these fine feature sizes?

Chester: Get in touch with your fabricator as early as possible and make sure you discuss this with them. They will have all kinds of insight on what to do and having them review your design as you progress will increase the chances of a Revision A success. They will also be able to give you additional details of their capabilities and any issue areas they have encountered on other previous designs.

Dunn: Thank you so much for talking with me today. **DESIGN007**

Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, click here.

MilAero007 Highlights

PRIDE Industries: A Nonprofit EMS and Staffing Firm Moves Into Mil-aero

PRIDE Industries is a contract manufacturing provider with a twist: The company provides training and coaching for job seekers with disabilities, including service-disabled veterans. If they don't have openings in their Sacramento facility, they may have a job for you in one of 15 other states.

New Views of Mars Thanks to Intel Tech

Earthlings can't get enough of the Red Planet. And unbeknownst to most—even to some of the engineers who've been involved (more on that later)—NASA's Mars 2020 Perseverance rover contains a vital piece of Intel-based tech that's helping get these images beamed back to us.

BSU Updates High-Performance X-ray Inspection Capability

BSU Inc., a growing EMS company, has updated its high-performance X-ray inspection capability with the installation of a Nikon XT V Series world-class X-ray and CT inspection system.

TTM Technologies, Inc. Reports Fiscal Q1 2021 Results

TTM Technologies, Inc., a leading global printed circuit board and radio frequency (RF) components and assemblies manufacturer, reported results for the first quarter of fiscal 2021, which ended on March 29, 2021.

Defense Speak Interpreted: Defense on Legacy Weapons Systems

As "Defense Speak Interpreted" readers have surmised, the weapons systems of yesterday, today, and tomorrow are under review, both with President Biden and with the Congress now in control by Democrats. But "weapons systems of yesterday"? In the fast-paced consumer electronics world, "legacy" never comes up.

Celestica Announces First Quarter 2021 Financial Results

Celestica Inc., a leader in design, manufacturing and supply chain solutions for the world's most innovative companies, has announced financial results for the quarter ended March 31, 2021 (Q1 2021).

Inmarsat, Honeywell Partner to Deliver Innovative SATCOM Solutions to the U.S. Government

Honeywell and Inmarsat, the world leader in global, mobile satellite communications, announced an agreement to develop and deliver innovative commercial satellite communications solutions to the U.S. government.

Lenthor Engineering Adds Joel Robbins as Business Development Manager

Lenthor Engineering, Inc., a California based designer, manufacturer and assembler of flex and rigid-flex printed circuit boards, has added Joel Robbins in the role of business development manager with primary responsibility for the South Central and South East territories.

Collins Aerospace Reaches Significant Milestone in its Iridium Certus Development

Collins Aerospace has reached another critical milestone in the development of its higher bandwidth Iridium Certus® airborne satellite communications (SATCOM) system.

Embedding Resistor Elements, Part 2

Designers Notebook

by Vern Solberg, CONSULTANT

The decision to embed passive components within the PCB structure is commonly prompted by two key barriers: restricted surface area and interconnect complexity. The PCB's functionality may also require a significant number of semiconductor packages, often requiring very close coupling to meet their target performance potential. Regarding surface area challenges, many companies are confronted with the need to reduce end-product size to maintain a competitive edge in a particular market, or to satisfy the anticipated needs of their customer base.

Over 70% of the components occupying space on a typical printed circuit board are passive (resistors, capacitors, inductors). Although most passive components are minimal in size, they can occupy up to 50% of the board's surface area. Transferring most of the resistor elements onto the subsurface layers of the PCB will enable the designer the opportunity to optimize semiconductor placement, reduce circuit board size (typical of that illustrated in Figure 1), and ultimately achieve the most efficient interconnect between principal functions.

As an alternative to the thick-film resistor process detailed in Part 1 of this topic, a significant number of PCB fabricators are offering embedded thin-film resistor capability. In comparing the thick-film resistor forming process, photo-lithography has replaced the printing and dispensing of paste-like resist materials to define the embedded resistors' geometry. Many circuit board fabricators prefer the coated copper foil technology because the composite material's base value range is more precise than the deposited thick-film alternative, ensuring that the value and tolerance of the formed resistor element is more likely to meet customer expectation.

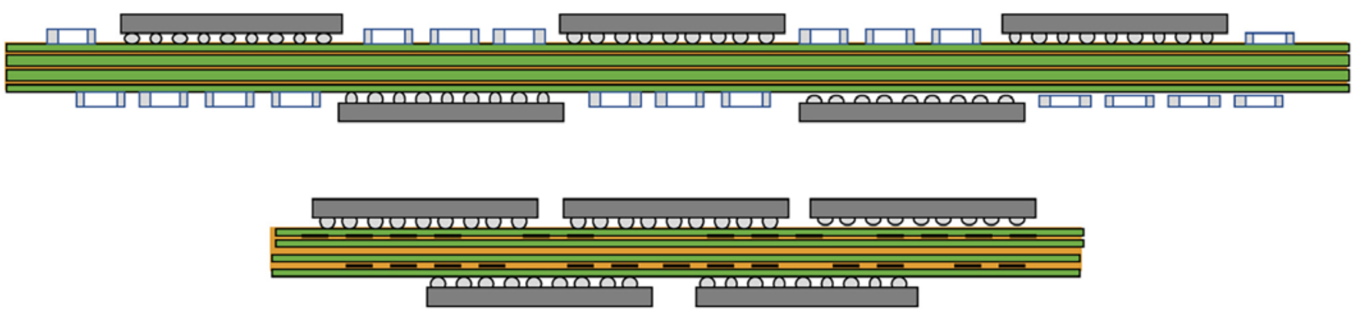


Figure 1: Comparing PCB area utilization of discrete surface-mounted resistors to that employing embedded thin-film resistors.

Base Materials for Thin-Film Resistor Forming

To begin, a resistive alloy coating is deposited onto copper foil to create the base material for embedded resistor applications. The resistive alloy is electrodeposited or deposited onto the copper foil using a roll-to-roll sputtering process. Resistive alloy thickness determines the overall resistance value (ohms/sq.) of the coated copper foil. Alloys commonly applied for embedded resistor applications include nickel phosphorous (NiP), chromium silicon monoxide (CrSiO), nickel chromium aluminum silicon (NCAS), and nickel chromium (NiCr). The sheet resistance of nickel-chrome alloy film containing 20% chromium, as an example, will furnish the designer with a resistance range as high as 3 K-ohms.

Resistor Element Planning

Typical of the discrete resistor element, the formed resistor will span the area between two copper lands. The shape of the resistance material between the copper lands can be a simple square, a series of squares to form a rectangle, or a shape designed to maximize resistor element length while minimizing area.

Initial planning:

1. Identify resistors for embedding.
2. Establish R-value and target tolerance.
3. Determine power rating requirement.
4. Define finished element geometry.
5. Select location (layer) and orientation.

The power dissipation is the rate at which resist energy is lost in elements. The power capability for embedded resistors will depend on the physical size of the resistor elements, temperature rating of the surrounding substrate materials, and the board stack-up. In the end it boils down to how the heat generated is managed. Typical power dissipation for most thin-film resistor designs operating at an ambient of less than 70°C is approximately 1/10 to 1/8 watt.

Typical of the thick-film composites, the base values of the thin-film resist-coated copper foil sheet materials are based on a single square geometry. While terminating resistor values are predominantly 50 ohms, and pull-up resistors fall in a range between 1K ohm and 10K ohm, these base values can be extended to furnish significantly higher resistor elements.

Implementation:

1. Establish land pattern (termination) geometry.
2. Define overall element dimensions.
3. Select optimum element position.
4. Plan most efficient circuit interface.
5. Provide features for test probe access.

As noted, the "square" geometry represents the basic ohm value of the resistive material. The designer can increase the resistance value by simply extending the length of the resistor pattern with additional squares or partial square segments (Figure 2).

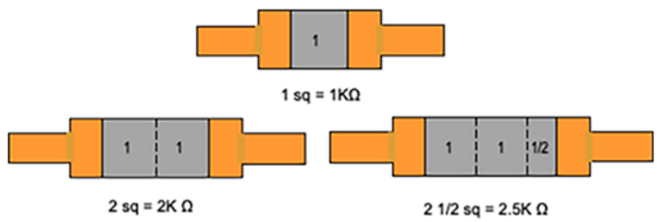


Figure 2: Basic "bar" resistor element design.

The resist-coated copper foil will become an integral part of the multilayer circuit board construction that, when processed, will furnish both formed resistor elements and provide general interconnect functions. The formed NiP resistor element examples (Figure 3) represent a subsurface interconnect layer prepared for lamination within a multilayer PCB.

After chemically removing copper and defining the resistor image, the now exposed nickel-phosphorous resistive material exhibits a matte grey finish.

To enable efficient utilization of the primary base value of the coated foils, the element

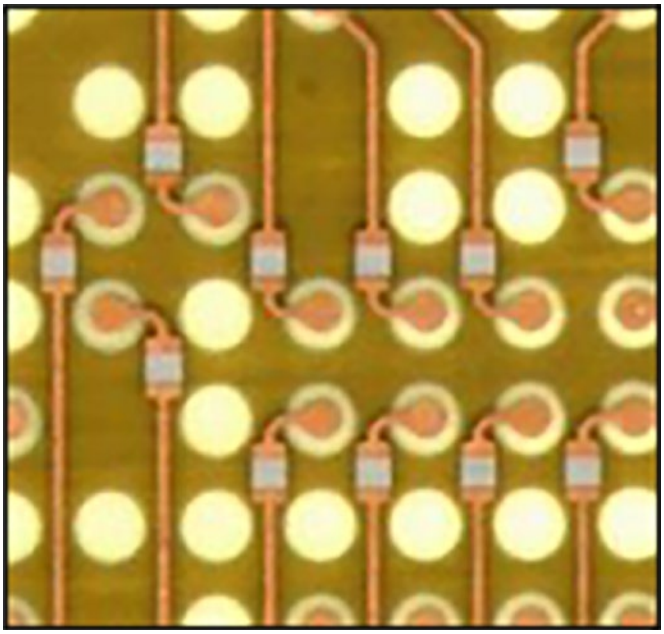


Figure 3: Subsurface conductor layer with formed thin-film resistors. (Image source: Ohmega Technologies, Inc.)

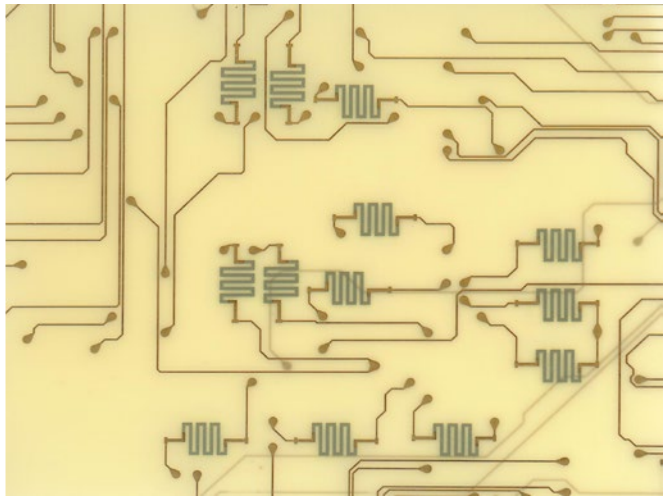


Figure 4: Serpentine-configured thin-film resistor examples. (Image source: Ohmega Technologies, Inc.)

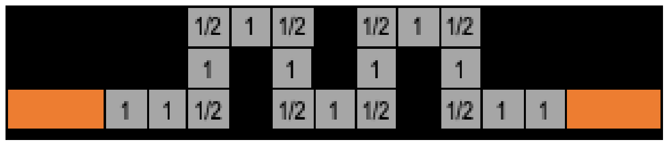


Figure 5: Serpentine resistor element design rules.

geometry can be extended further in length to provide a broad range of resistor values. When the resistor element length becomes too long, however, it can restrict or block efficient circuit routing paths. To compress the surface area required for the more complex resistor elements, it is common practice to compress the physical area using a "serpentine" configuration typical of that exhibited in Figure 4.

The design rules for the serpentine-configured resistor pattern are significantly different than the straight bar configuration detailed above. When developing the resistor element in a serpentine configuration the designer must adjust the basic value at each corner of the serpentine pattern. The square geometry located at each corner transition will furnish a value that is only one-half the resist material's base value. The 19-square resistor pattern illustrated in Figure 5 represents a 15K-ohm resistor utilizing 1K-ohm base value material.

Regarding individual resistor tolerance control, thin-film material suppliers note that most circuit board fabricators will anticipate a resistor tolerance at or less than 20%. The resulting tolerance will be dependent on the precision of the image and etch process. Precise etch control will repeatedly produce resistors with a tolerance range encompassed by what the fabricator can maintain on controlled impedance lines and the published sheet tolerance. Variation of the tolerance can be minimized by maintaining a uniform element width (≥ 200-micron) for the resistor patterns and fine-tuning the resistor element length to achieve the required target resistor value. But the designer must keep in mind that over specifying resistor tolerance will likely impact processing costs.

Sourcing Thin-Film Resistive Materials

Resist coating can be furnished on any copper foil thickness, but thicknesses of 12 µm, 18 µm (0.5 oz) and 35 µm (1 oz) are likely to be more available because they are commonly selected for a wide range of multilayer organic circuit board applications. The two leading suppliers of the copper foils furnished with the resistive coatings in North America

Resistive Material (alloy composition)	NiP	NiP	NiP
Sheet resistance (Ω/sq.)	10	25, 40, 50, 100	250
Sheet resistivity tolerance	+/- 3%	+/- 5%	+/- 10%
Thermal coefficient of R (ppm/ºC)	+/- 100	-20	300
Copper foil thickness (microns)	18, 35	18, 35	18, 35
Foil maximum width (mm/in)	1295/51	1295/51	1295/51
Maximum power dissipation at 40ºC	10Ω/sq.:250	25Ω /sq.:250 40Ω/sq.:225 50Ω/sq.:200 100Ω/sq.:150	1KΩ/sq.:100

Table 1: Ohmega Technologies resistive sheet materials.

are Ohmega Technologies LLC. and Ticer Technologies.[1]

Materials provided for resistor formation from Ohmega Technologies are described as a subtractive technology where the base material preparation begins with a thin-film resist-coated copper foil laminated onto a glass-reinforced dielectric. In preparation, the company first electrodeposits a thin coating of nickel phosphorous (NiP) alloy onto the copper foil's matte or tooth side. Base resist values of the Ohmega coated copper foils range from 10 Ω/sq. to 377 Ω/sq. (Table 1).

The power dissipation is the rate at which resist energy is lost in elements. The power capability for embedded resistors will depend on the physical size of the resistor elements, temperature rating of the surrounding substrate materials, and the board stackup. In the end it boils down to how the heat generated is managed. Typical power dissipation for most thin-film resistor designs operating at an ambient of less than 70 °C is approximately 1/10 to 1/8 watt.

Coated foil materials can be furnished as a foil only product or pre-laminated to a variety of standard FR-4, polyimide, or more specialized microwave substrate materials. The pre-laminated material can be furnished directly from Ohmega Technologies as well as other sources, including Arlon, Rogers, and Taconic. The company also offers a NiP material with a sheet resistivity of 377 ohms per square, which was developed for a range of specialized applications that include high impedance and frequency selective surfaces, antenna arrays, or as radar absorbing materials for resistive cards.

Three variations of resistive-coated thin-film on copper foils are available from Ticer Technologies that provide a specific range of resist coatings: nickel-chromium (NiCr), nickel chromium-aluminum-silicon (NCAS) and chromium-silicon-monoxide (CrSiO). Individually, these alloy compositions can furnish a broad range of base resist values from 25 ohms to 1K ohms. Table 2 details the sheet resistance value range, tolerance and the maximum power dissipation factor for the three resistance alloy compositions noted.

Ticer Technologies resistive-coated copper foil material is furnished in sheet form or as a product pre-laminated onto standard ROHS-compliant FR-4 glass-reinforced resin material

Resistive Material (alloy composition)	NiCr	NCAS	CrSiO
Sheet resistance (Ω/sq.)	25, 50, 100	25, 50, 100, 250	1000
Sheet resistivity tolerance	+/- 5%	+/- 5%	+/- 7%
Thermal coefficient of R (ppm/°C)	< 110	-20	300
Copper foil thickness (microns)	18, 35	18, 35	18, 35
Foil maximum width (mm/in)	1295/51	1295/51	1295/51
Maximum power dissipation at 40°C	25Ω/sq.:250 50Ω/sq.:200 100Ω/sq.:150	25Ω /sq.:250 50Ω/sq.:200 100Ω/sq.:150 250Ω/sq.:75	1KΩ/sq.:250

Table 2: Comparing Ticer Technologies resistive coating characteristics.

or any number of reinforced specialty resins from a vast network of global material suppliers.

Resistor Process Sequence

The resistor forming process will include two or three etch steps, depending on the resistor alloy selected. The process flow illustrated in Figure 6 from Ticer Technologies represents a two-stage chemical etching sequence for their nickel chromium (NiCr) resistive material.

With respect to circuit layer preparation, fabricators are able to image and chemically

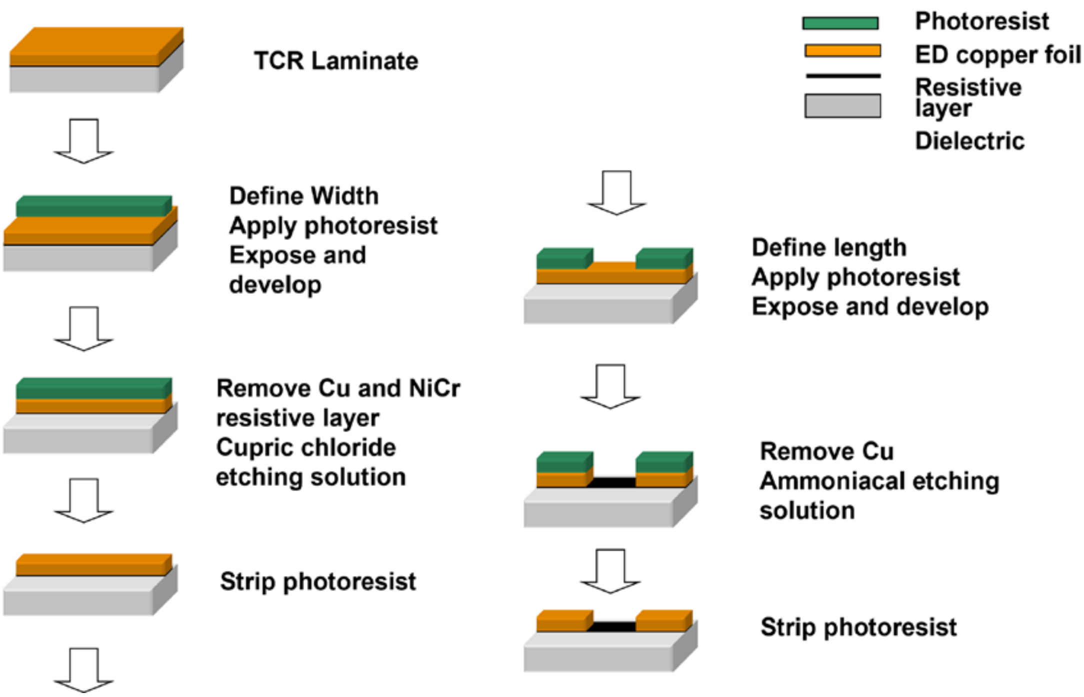


Figure 6: Thin-film resistor forming process sequence.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etch the circuit layers using standard subtractive PCB processing. As far as chemistry, the printed circuit board industry commonly employs cupric chloride etchants for the primary circuit image and resistive layer width definition. A second etch step is required to selectively remove copper to define the length of the resistor elements. This process requires a different chemistry to ensure only copper removal without altering or degrading the remaining resistive element geometry.

Power Dissipation

As far as handling power, the manufacturers state that power density is defined as the total power dissipated divided by the effective surface area. The power density of the resistor element increases as the area decreases. All other conditions illustrate that for the same power input, the temperature rise will depend on the area of the resistor. In other words, the resistors with a larger surface area can dissipate more power than a narrow geometry, provided that all conditions remain the same. If space is available, design the resistor element to be as wide as possible. Additionally, when the resistors are buried within the layers of the circuit board, the physical and thermal characteristics of the substrate material (the total thickness of the substrate and the collective number of copper layers) will directly affect heat dissipation from the fully assembled circuit board.

Omega Technologies notes that electrical current should not exceed the rated current-carrying capacity of the resistor because excessive current could cause permanent damage to the formed resistor element.[2]

In-Process Testing

Prior to further circuit layer lamination, the resistor elements' value and tolerance must be validated. The "flying probe" test is widely used to validate the embedded resistor elements' target value before lamination of additional circuit layers. Most flying probe testers can also perform signal integrity testing as well as identify the location of opens and shorts. To enable test probe access, dedicated land features must be provided for each formed resistor element. Lands provided for test probe access must not be arranged in a way that would require probes to cross over or contact other probes. When laser trimming is required to fine-tune a resistor element, the probe contact must not interfere with laser access while making a trim. For best test and trim accuracies, the test lands should be near to the resistor-to-circuit termination point to ensure precise resistor value measurement.

When developing land geometry for test-probe access, probe tip shape and dimensions will determine the minimum land size. Test system manufacturers state that probes have a placement tolerance of 50 µm (0.002") in each of the X, Y, and Z axes. The land pattern diameter must be greater than the probe tip to accommodate probe positional tolerances and allow for uniform probe pressure and pad scrub. First-time users should refer to their circuit board supplier to determine the suitability of their test equipment and availability of the required software for testing the embedded resistor elements.

Design Tools

Most software developers are currently furnishing the necessary tools to implement the embedded resistor elements within the multilayer circuit board. Material suppliers suggest that the CAD designer consider using Mentor, Allegro, Intergraph, and PAD Power PCB in conjunction with an Excel program to aid in developing the more complex resistor element geometries. While several resistor elements will likely remain on the outer surface of the finished circuit board, the embedded resistors will require a unique reference designator to avoid procurement errors. For example, a surface-mounted resistor will be defined as R110 while the embedded or buried resistor will be labeled BR110 on the schematic diagram and material list.

Implementation Issues and Concerns

Formed passive resistor element values and tolerance that range between 5–10% will likely meet the operational criteria of the final product but altering the value after lamination will not be an option. Due to the physical stresses experienced during PCB lamination and assembly processing, target values of resistors may drift outside the specified resistance target, and laser trimming will not be practical. When the specified values of the resistor elements require tolerance in the 1-2% range, I strongly advise the circuit board designer to retain these higher precision resistors as discrete surface mount components for placement onto the circuit board's outer surface(s). **DESIGN007**

References

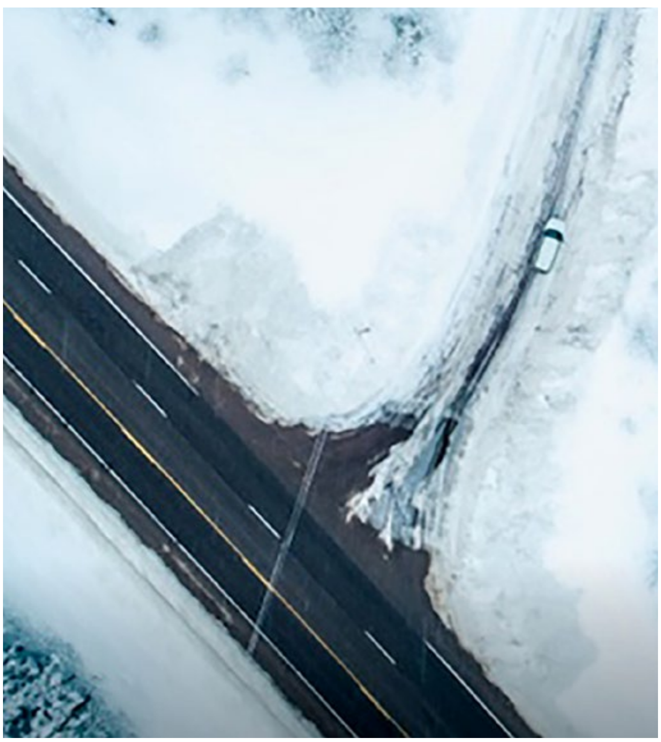
1. Ohmega Technologies has been acquired by Quantic Electronics, a business unit of Arcline Investments which focuses on specialty component materials. More recently, Quantic also acquired Ticer Technologies. The company stated that it plans to maintain multi-plant resistive foil operations for both OhmegaPly and Ticer TCR materials.

2. For more information refer to the *Power Dissipation Guidelines* contained within the Resistor Calculators on both Ticer's and Ohmega's websites.

Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. Read part one of this column, "The 'New and Growing' Embedded Resistors." To read past columns or contact Solberg, click here.

Driving in the Snow is a Team Effort for AI Sensors

A major challenge for fully autonomous vehicles is navigating bad weather. Snow especially confounds crucial sensor data that helps a vehicle gauge depth, find obstacles, and keep on the correct side of the yellow line, assuming it is visible. Averaging more than 200 inches of snow every winter, Michigan's Keweenaw Peninsula is the perfect place to push autonomous vehicle tech to its limits. In two papers presented at SPIE Defense + Commercial Sensing 2021, researchers from Michigan Technological University discuss solutions for snowy driving scenarios that could help bring self-driving options to snowy cities like Chicago, Detroit, Minneapolis and Toronto.

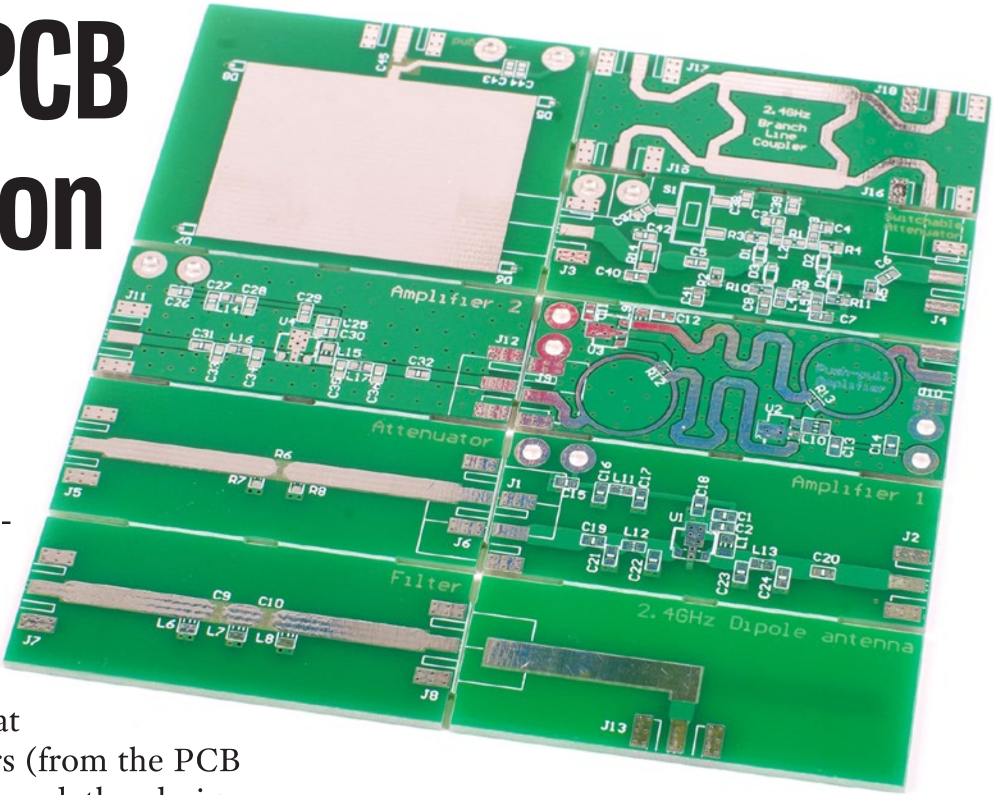


Since artificial brains aren't around yet, task-specific AI algorithms must take the wheel—which means autonomous vehicles must rely on multiple sensors. Fisheye cameras widen the view while other cameras act much like the human eye. Infrared picks up heat signatures. Radar can see through the fog and rain. Light detection and ranging (lidar) pierces through the dark and weaves a neon tapestry of laser beam threads. Using sensor fusion, Rawashdeh and Bos want autonomous sensors to collectively figure out the answer—be it elephant, deer, or snowbank. As Bos puts it, "Rather than strictly voting, by using sensor fusion we will come up with a new estimate."

While navigating a Keweenaw blizzard is a ways out for autonomous vehicles, their sensors can get better at learning about bad weather and, with advances like sensor fusion, will be able to drive safely on snowy roads one day.

(Source: Michigan State University)

DFM 101: PCB Panelization



Article by Anaya Vardya
AMERICAN STANDARD CIRCUITS

Introduction

One of the biggest challenges facing PCB designers is not understanding the cost drivers in the PCB manufacturing process. This article is the first in a series that will discuss these cost drivers (from the PCB manufacturer's perspective) and the design decisions that will impact product reliability.

DFM

Design for Manufacturing (DFM) is defined as the practice of designing printed circuit boards that meet not only the capabilities of the customer's assembly manufacturing process, but also the capabilities of the board fabrication process at the lowest possible cost. While not a substitute to early design engagement with the PCB fabricator, these articles will provide guidelines that will help to "design for success."

SPECIFICATIONS	STANDARD	ADVANCED
Panel sizes, multilayer	12x18, 18x24, 21x24	20x32
Panel sizes, double sided	9x12, 30x30, 18x36	
Number of layers	<=16	>16
Layer-to-layer registration	0.003	0.0005
Foil types available	CAC, ED Copper	

Table 1: Several different standard panel sizes are typically available, as well as custom-sized panels for large footprint applications, and custom design and special tooling (all units in inches).

Panelization

Panelization is the process of placing one or more printed circuit boards (PCBs) on a manufacturing panel and incorporating features to assist manufacturing (such as tooling holes, fiducials, coupons, panel thieving, etc.). Panelization is one of the highest-impact factors in the cost of a PCB.

The panel area available for circuit boards and coupons is known as the usable area. The number and type of coupons are based on the specs that the PCBs are being built to and requirements for controlled impedance. Coupons may sometimes further reduce the amount of a PCB panel that is available for the circuit boards. This area is measured as a percentage, defined by the total area for PCBs divided by the total panel area.

PCBs are arranged in the useable area. Any area outside the useable area is designated for tooling to optimize manufacturing or

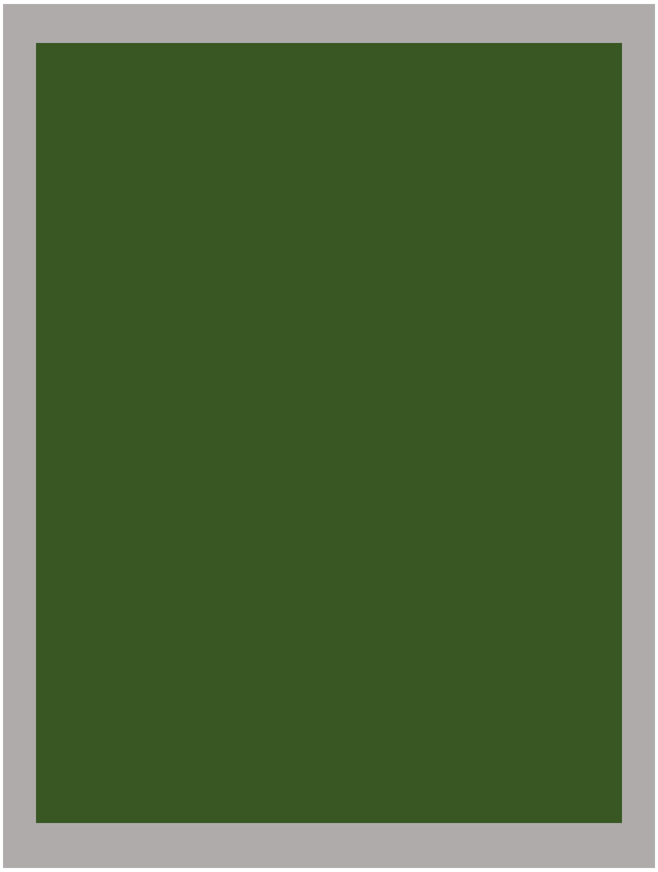


Figure 1: The panel area available for circuit boards and coupons is known as the usable area.

in-process inspection tools such as line width checks and coupons.

Cost-effective material utilization is defined by a target panel with greater than 75% panel utilization.

Raw laminate is the primary cost constituent of a multilayer PCB. Optimizing panel structure around standard base materials while achieving maximum material utilization on standard panel sizes can have a significant impact on multilayer board prices and deliveries. The three most preferred sizes are 12x18 inches, 18x24 inches and 21x24 inches. The most effective cost per unit area processed is typically found with larger panel size. The most common panel size is 18x24. For special applications, other panel sizes are provided.

The most effective material utilization will be achieved with PCBs or arrays of PCBs where their finished outline fits as efficiently as possible within the useable area of the panel. Test coupons must be within the useable area. The customer may negotiate to have locating holes and/or breakaway tabs for the insertion or surface mount equipment located outside the useable area. This is usually accomplished via the tab-routing process. Material utilization may be increased by employing the scoring process. This process places grooves on opposite sides of the panel between boards for snapping the boards from the panel. This method allows boards to be butted up against each other, eliminating the real estate for rout paths, thereby allowing more boards to be placed on the panel.

For single- and double-sided product, a 0.500" border is required around the periphery of the panel for tooling purposes. For multilayers, this allowance is 0.750." Work with your PCB fabricator to design the most cost-effective array/panel layout for your application.

Panel Usable Area

The following table can be used to determine the maximum, single 1-up PCB that can fit into a panel. Panel sizes are subdivided into "standard" (most common) and "optional" (custom) classifications.

There are three general modifications to a panel that will reduce the available usable area:

1. Step-and-repeat requirement.
2. Provisions for electroplating edge connectors.
3. Coupon requirements such as MIL spec or impedance.

Step-and-Repeat

This is the process of reproducing successive images onto a panel. For PCBs without gold-plated edge contacts, the standard step-and-repeat spacing between parts is normally 0.100."

Controlled Impedance Coupons

PCBs with controlled impedance technology are processed with test coupons as part

TYPE	PANEL SIZE	USABLE AREA	
		DOUBLE/SINGLE SIDED	MULTILAYER
Standard	12x18	11x17	10.5x16.5
Standard	18x24	17x23	16.5x22.5
Standard	21x24	20x23	19.5x22.5
Optional	9x12	8x11	N/A
Optional	30x30	29x29	N/A
Optional	18x36	17x35	N/A

Table 2: Panel sizes are subdivided into "standard" (most common) and "optional" (custom) classifications (units in inches).

of the lay-up. Typically, an additional one-inch border area is required. When a 20% or less nominal impedance tolerance is specified, using controlled geometry coupons is recommended to ensure values are met.

MIL-SPEC Coupons

Any PCBs requiring MIL Spec conformance will require a MIL Spec coupon be placed on each PCB. Typically, an additional one-inch border area is required.

Assembly Rails

The following should be considered to maximize the number up on a panel when assembly rails are required. A minimum of a 1.0" border typically must be maintained around the perimeter of the panel to allow for pinning, coupons, plating clamps, and other assorted targets that are required to tool a panel. It is a common practice to allow the assembly rail (breakaway) to protrude into the 1.0" border by 0.5" to keep the PCB away from the border. When the rail enters the 1.0" border of the panel, some tooling features may remain on the rail after processing. This can include tooling holes, targets, inner layer gates, and thieving. These additional features do not affect any assembly operations.

Assembly Arrays or Sub-panels

PCBs are often required to be step-and-repeated onto an array for assembly. The assembly array database should be provided to your PCB fabricator to ensure that the correct array is provided to the assembler. The follow-

Figure 2: Understanding the cost drivers in PCB fabrication and early engagement between the designer and the fabricator are crucial elements that lead to cost-effective design success. Following your fabricator's DFM guidelines is the first place to start.

ing assembly panel attributes are required to properly define the assembly array:

1. 1-up PCB data.
   - Hole to board edge dimension
   - Board size
2. Array information.
   - Array drawing number
   - Array physical size
   - Rail dimensions
   - #-up in array
   - Depanelized
   - Can PCB fabrication tooling be located within rail borders?
3. Are there any components overhanging off the edge of the board?
   - If "yes," indicate location and dimension on a drawing
4. Does the board need to be in a specific orientation in relation to the array?
5. If there are multiple part numbers in the same array, locations and orientations must be specified. **DESIGN007**

Anaya Vardya is president and CEO of American Standard Circuits; co-author of *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals;* and author of *Thermal Management: A Fabricator's Perspective.* Visit I-007eBooks.com to download these and other free, educational titles. He also co-authored *"Fundamentals of Printed Circuit Board Technologies."*

BOOK EXCERPT

'The Printed Circuit Designer's Guide to... Thermal Management: A Fabricator's Perspective,'

Chapter 3: Metal-Core Boards

Conceptually, a metal-core board is exactly like it sounds—the metal is in the middle of the PCB sandwiched between layers on both sides. Just about any PCBA that will contain active heat-generating components can benefit when designed on a metal-core PCB. On a conventional PCB, the standard FR-4 layers are relatively poor thermal conductors, and heat is normally dissipated from active components using vias and thermal pads, as discussed earlier. A metal core has much greater thermal conductivity, allowing it to easily dissipate heat away from active components. This prevents hot spots that can form in PCBs by dissipating heat evenly across the PCB and increasing performance and lifetime.

One example would be in the LED lighting industry, where LEDs produce a significant amount of energy and heat. A metal-core PCB has two benefits in this application: it provides some natural reflectivity for any light that travels toward the substrate, increasing the device brightness; and the other is extending the life of the product by quickly transferring heat away from the LEDs.

Metal-core PCBs usually have blind via layers located on both sides of the metal-core substrate. There are also PTHs going through the entire package. From a PCB perspective, it is important to isolate the metal from the through-hole; otherwise, the board would short out completely. To accomplish this, one must start out by drilling the metal core approximately 40–50 mils larger than the PTHs, slots, or cutouts. It then needs to be filled with a non-conductive epoxy filler and then pressed.

After pressing the metal core, it then needs to have the filler compound removed from the surface and prepared for lamination with the inner layer cores. After lamination, the PTHs are drilled and processed through normal manufacturing processes.

Click here to download this free book.

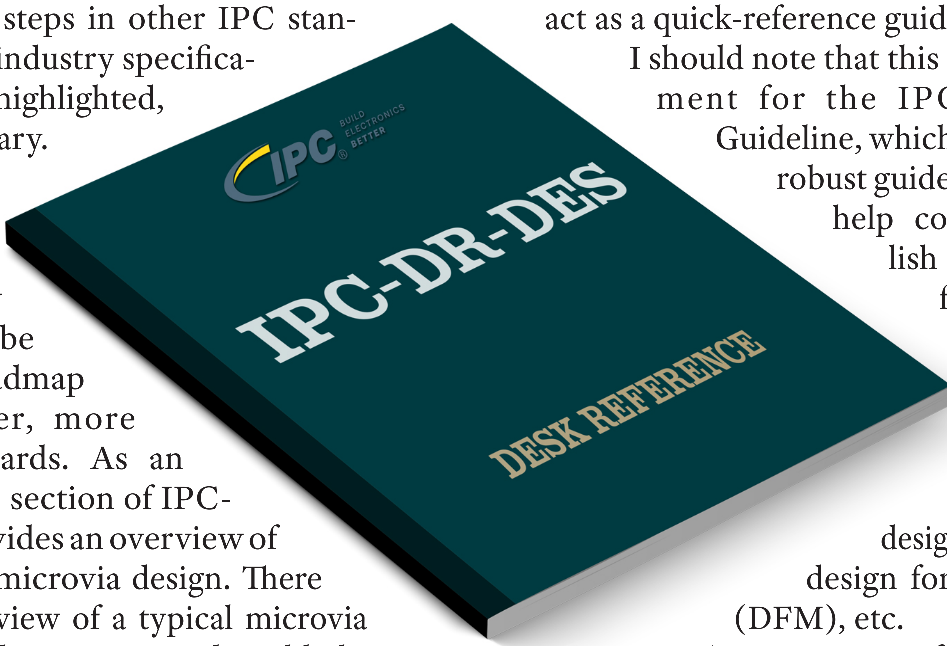
The IPC PCB Design Desk Reference is on Its Way

Design Circuit

by **Patrick Crawford**, IPC

Last month, a group of industry experts met to review and finalize IPC-DR-DES, a PCB Design Desk Reference created to help designers and engineers understand the requirements and critical parameters of IPC design standards. While I have referred to this project in previous columns, it is now in final draft, and I can write about it in more detail.

IPC-DR-DES guides its user through key steps in the design process—materials selection, stackup designs, pad stack designs, microvia design, solder mask, via protection, and tolerancing—and highlights where parameters and requirements can be found for those design steps in other IPC standards. Other industry specifications are also highlighted, where necessary.



As a Desk Reference, this document is only intended to be a tool—a roadmap toward other, more robust standards. As an example, one section of IPC-DR-DES provides an overview of laser-drilled microvia design. There is a cutaway view of a typical microvia with critical dimensions, and a table listing those parameters and where they can be found. In the case of laser-drilled microvias, there are a few parameters fixed by calculation (which are described elsewhere) and a few defined in IPC-6010. Other parameters are restricted by design decisions made elsewhere, and the table refers the user to those relevant sections in IPC-DR-DES.

The document is only 20 pages long in its current form and, if it isn't obvious, is intended to fit snugly on the desk of any designer or engineer designing or building boards to IPC specs. For a designer who is entering the industry, especially in emerging markets abroad, the IPC-DR-DES is intended to be a foundational pointer to other standards. For veterans, it can act as a quick-reference guide.

I should note that this is not a replacement for the IPC-2231A DFX Guideline, which is a much more robust guideline intended to help companies establish best practices for board design and the subsequent associated engineering processes: design for test (DFT), design for manufacturing (DFM), etc.

The intention is for the IPC-DR-DES to be revised or reaffirmed annually, as it refers to many IPC and industry stan-

dards that may undergo revision at any time. Additionally, new material can (and absolutely should) be added upon request by industry. Indeed, a quick turnaround is expected; as a Desk Reference, this document is not metered by the usual IPC Standards Development processes and can therefore be revised quickly. However, if the document is to be maintained annually, it is critical for continuous input from industry.

Last month, I worked with I-Connect007 to advertise the IPC-DR-DES working group and hopefully attract industry volunteers to make sure that this document is a relevant and useful product for the electronics manufacturing industry. I could not be happier with the response, and it is heartening to see design engineers from around the world volunteer their time.

So, I will leave this abbreviated column with a similar call to action: If you would like to become involved with IPC-DR-DES, please reach out to me. Alternatively, if you have an idea for a standard or other project that IPC can help make a reality, we have launched a new portal for submitting such ideas on IPC.org. To submit an idea or look at other ideas (and become involved), click here.

I look forward to hearing from you. DESIGN007

Patrick Crawford is the manager of design programs and related industry programs at IPC. To read past columns or contact him, click here or email PatrickCrawford@ipc.org.

Thin Is Now in To Turn Terahertz Polarization

It's always good when your hard work reflects well on you. With the discovery of the giant polarization rotation of light, that is literally so.

The ultrathin, highly aligned carbon nanotube films first made by Rice University physicist Junichiro Kono and his students a few years ago turned out to have a surprising phenomenon waiting within: an ability to make highly capable terahertz polarization rotation possible.

This rotation doesn't mean the films are spinning. It does mean that polarized light from a laser or other source can now be manipulated in ways that were previously out of reach, making it completely visible or completely opaque with a device that's extremely thin.

The unique optical rotation happens when linearly polarized pulses of light pass through the 45-nanometer film and hit the silicon surface on which it sits. The light bounces between the substrate and film before finally reflecting back, but with its polarization turned by 90 degrees.

The discovery by lead author Andrey Baydin, a postdoctoral researcher in Kono's lab, is detailed in Optica. The phenomenon, which can be tuned by changing the refractive index of the substrate and the film thickness, could lead to robust, flexible devices that manipulate terahertz waves.

Because terahertz radiation easily passes through materials like plastics and cardboard, they could be particularly useful in manufacturing, quality control and process monitoring. They could also be handy in telecommunications systems and for security screening, because many materials have unique spectral signatures in the terahertz range, Kono said.

(Source: Rice University)

Thermal Management—
Good Design Practice for Heat Dissipation

Sensible Design

by Jade Bridges, ELECTROLUBE

Trial and error is an essential process in the development of new and innovative products, however, excessive testing can be unnecessary and costly. Incorporating thermal management at the preliminary stage of your design process will ultimately lead to more reliable and cost-effective end products. As a matter of good practice, evaluating thermal performance in all phases of the design cycle will also confirm any issues early on and help to prevent a costly system-level teardown.

This month, I'll be exploring thermal management tips for effective heat dissipation at the design stage as well as examining helpful tools to protect your electronic circuitry. Let's explore some of these key areas in more detail and discuss good design practices that ensure better thermal management.

Good Design Practice

The following list contains some of the key factors. How important are these and are there additional ones?

- Performance data and dimensions of the components
- Major heat-dissipating components
- Size of the PCB
- PCB material, layout, and component placement
- Mounting peripherals
- Temperature of the application environment
- Amount of heat dissipated
- Appropriate cooling methods, i.e., cooling fans, heat sink, etc.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See How

All the above points could influence the efficiency of the design produced and there are arguments for the importance of each one. In my opinion, you can separate these out into two categories, with high priority items including the correct choice of materials, the overall layout of the PCB, and the temperature of the surrounding environment. Factors such as the overall size of the PCB, the amount of heat dissipated, and the mounting peripherals are perhaps less important because they will all be dependent on the design; in some cases, they may have a large impact and in others, a negligible effect. The main point is that none of these factors should be considered alone. To achieve good thermal management, a holistic approach must be taken with suitable thermal analysis to ensure the best overall performance is being achieved.

To achieve good thermal management, a holistic approach must be taken with suitable thermal analysis to ensure the best overall performance is being achieved.

Identifying Components

Is it possible to identify components with the potential to dissipate more heat and factor this into the design process?

By reviewing the power consumption of components, you may get an indication as to the potential heat generation of a component, but this is not an ideal method to use. Each PCB will be designed differently and have an array of components. It is how these components interact with one another and how heat can flow through the assembly that should be considered in detail during the design phase. For example, heat-sensitive components should not be placed next to components with high heat generation. Components with higher power consumption should be placed near heat-dissipating technologies. Wherever possible, a relatively even heat distribution should be maintained rather than having "hot" and "cold" areas of the board. Using heat dissipating technologies, such as thermal interface materials, can assist in achieving this successfully.

Thermal Analysis Tools

What thermal analysis tools exist to identify thermal problems with a PCB?

At a basic level, thermocouples can be used to measure the temperature of specific components or areas of a PCB. More recent technologies consider the use of heat flow sensors to show the movements of thermal energy throughout the board and specifically through components. They can be used to show the generation of heat by a specific component, and the ability of the component to absorb heat generated by an external source. Thermal imaging can be used in a similar way to show the various temperatures across PCBs. Infrared cameras also carry out thermal imaging of the board and individual components. They can give a clear view on where heat is gathering within the device and help to show where additional heat dissipation may be required.

Removing Heat

What are the most common methods to remove heat from circuit boards?

Heat dissipation can be achieved in a number of ways. As we have already discussed, the design of the PCB can help to manage the heat flow across the board and ensure successful heat dissipation. Where heat generating components are present, a heat sink and thermal interface material may be effectively utilised. In addition, if thermal analysis shows that there are still areas of the PCB where heat may be gathering, thermal gap-filling compounds may offer additional heat dissipation. In other technologies, forced air flow and fluid cooling may also be used, however, these may not be suitable for all devices as they may require extra space or technology to successfully implement. This again shows the flexibility of thermal management compounds that can be used at the interface of a component and heat sink device, thus improving heat dissipation from the source.

Heat dissipation in compact electronic assemblies is a vital design issue, which, if not fully appraised at the design stage, could cause premature product failure and loss of supplier reputation. Most electronic components are low power and produce negligible amounts of heat in their operation, however some devices, such as LEDs, power transistors, CPUs, and power diodes produce a significant amount of heat. Failure to effectively dissipate this heat away from the component or device can also lead to reliability concerns and reduced operational lifetimes. Sufficiently implementing thermal management at the early design phase and evaluating it from concept to manufacturing will create reliable devices with an extended life expectancy. There's a lot to consider when selecting the appropriate thermal management material, however, our technical support team can help designers find the right solution for specific heat transfer challenges. I hope this column has been useful and of course, we are always happy to help and advise. In the meantime, watch for my next column on thermal management. **DESIGN007**

Jade Bridges is global technical support manager at Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch the micro webinar series "Coatings Uncoated!"

ICAPE Group Offers Boots on the Ground Support in Asia

Nolan Johnson speaks with Roger Harts about some of the current complications around manufacturing electronics in China and how ICAPE Group works as a vital supplier partner to OEMs and companies hoping to manufacture in Asia. Harts is the director of ICAPE USA and has been for the last five years. ICAPE USA is a member of ICAPE GROUP, a global printed circuit board company, also manufacturing custom-made technical parts. According to Harts, with roughly 2,500 customers, ICAPE delivers 22 million circuit boards a month, and another five million custom-made technical parts.


Roger Harts

Johnson: We wanted to focus on ICAPE Group's work in China. Let's start with an overview; what's happening in China for ICAPE Group?

Harts: Even though our corporate headquarters is in Paris, France, our largest office is in Chang'an, just outside of Shenzhen, where we have over 250 people working in different departments such as engineering, purchasing, laboratory testing, quality, logistics, etc. Because of the pandemic it's very difficult to travel to China, to audit factories and maintain working relationships, but because of the size of our office in China, we can provide those types of services to customers. Prior to the pandemic, we flew in a lot of people to tour facilities and offices, and we worked with them to audit factories as well. Our China office has become a true advantage. In fact, it is the largest office for any company with a similar business model.

Click here to continue.

Star Trek Memories

Flexible Thinking

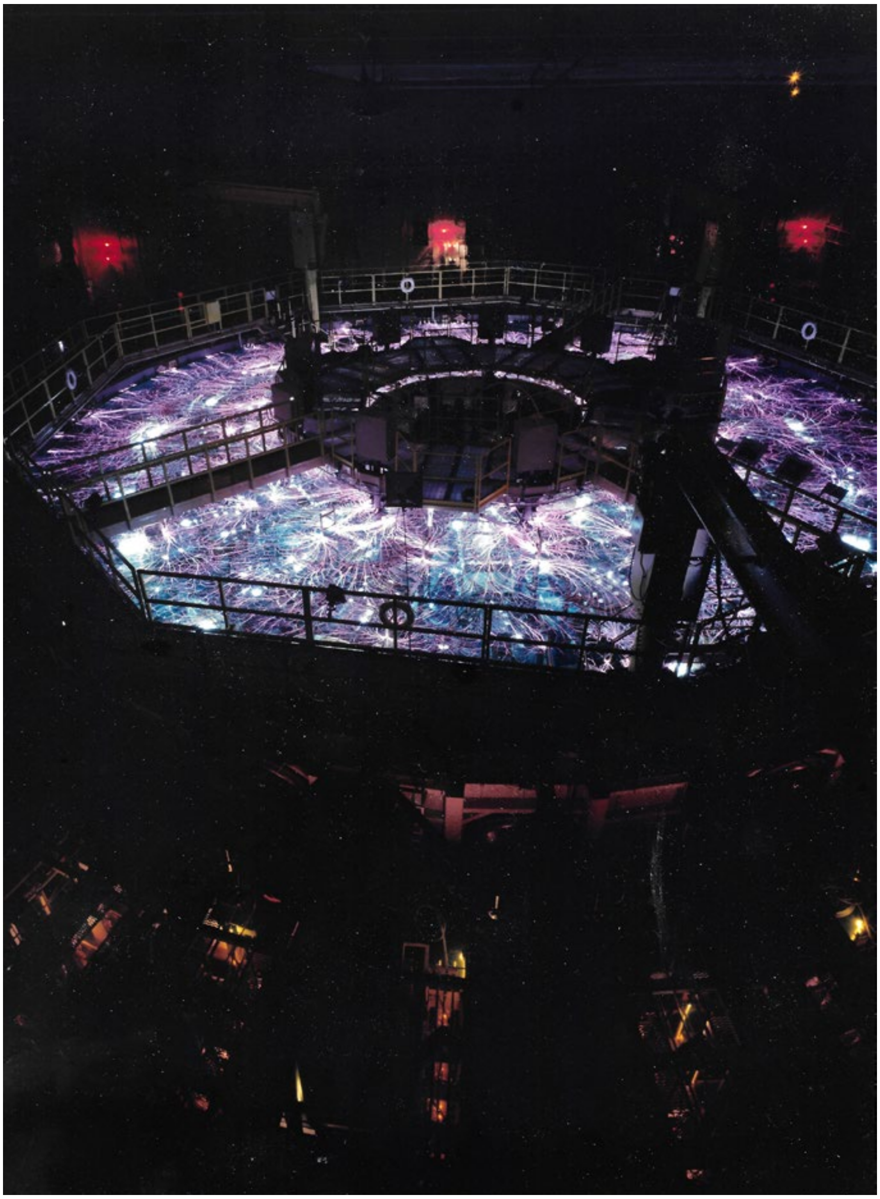
Feature Column by Joe Fjelstad, VERDANT ELECTRONICS

I am one of the few regular I-Connect007 contributors who is old and privileged enough to have watched the original *Star Trek* series in 1966. Contemplating this has stirred up memories of my childhood and early interest in science. I spent my early years with my father, an airplane enthusiast and aerospace engineer with Lockheed Martin who worked on the F-104 flight instrumentation, and who took his family out to see flight demonstrations at Edwards Air Force Base where he worked.

You can say I got hooked early on space travel. I remember looking up from the playground during recesses as the nation took its first steps into the space age and manned space flight. The X-planes routinely shattered the sound barrier and disappeared into the sky above in Lancaster, Calif., where my family lived. I was one of those pesky kids with too many questions, bothering the neighborhood menfolk with my questions. My targets were many and diverse: engineers like my dad, a couple of test pilots, and even an FBI agent for good measure. The passion for flight, especially rocketry, entered my veins early.


Joe Fjelstad (center) at his high school graduation with his parents, Marjorie and John Fjelstad.

Soon came actual space flight and it seemed like a fantasy. First was Yuri Gagarin of the Soviet Union, followed by Alan Shepard, the first American in space. Space was very risky business and the engineers at NASA and elsewhere were making it up "on the fly," so to speak. Following a brief but harrowing brush with a possible nuclear apocalypse



Particle Beam Fusion Accelerator firing in the 1980s. (Source: Sandia National Laboratory)

during the Cuba Missile Crisis, the nation recaptured its breath and its progress in space travel continued.

At that time, my father was working for Lockheed on the RM-81 Agena Target Vehicle, also known as the Gemini-Agena Target Vehicle, a spacecraft without crew used by NASA during its Gemini program to develop and practice orbital space rendezvous and docking. Later, my father also worked on the Space Shuttle's engines at Rocketdyne and it afforded me a 1976 visit to my folks in Canoga Park. We visited the assembly building in Palmdale, California, with my father where the first shuttle, the Enterprise, was being finished and the Columbia was in progress. (Members of the *Star Trek* cast had been there a few months earlier to see the Enterprise).

However, turning back a decade to 1966 to when I was in high school in Santa Clara Valley, the area was known as "Valley of the Heart's Delight" and not yet "Silicon Valley." That was the year *Star Trek* was first broadcast and I was joining my friends in building homemade rockets. This included making the engines and our own rocket fuels, which I cooked on the family stove and which cost my dear mother one of her favorite pans when I decided the easiest way to clean the residue from it was to burn it out (bad idea).

My favorite collaborator friend and I used to watch the new series on his family's color TV as he had control of the TV for that hour every week and I didn't. It was a departure from the normal fare and the creativity of the writers was showcased weekly. We marveled at the technical wizardry that would be available in 200 years hence in the year 2265. As it turned out, a number of those futuristic devices made appearances well before that date. Perhaps the most notable was the Motorola flip phone which was reportedly modeled after the *Star Trek* "communicator" design. I did not know then that I would one day be making flex circuits for prototype products that would be mimicking what was shown on the screen. The tricorder was another device that has modern parallels such as ultrasound imaging—another technology facilitated by flexible circuits—

which sends and receives data by means of a piezo transducer head. Other devices with *Star Trek*-like technology I helped build circuits for in the mid-1980s included the plasma opening switch for the Particle Beam Fusion Accelerator (PBFA) fusion power investigations at Sandia National Labs, and elements of early LED displays that were the precursors of today's flat-screen TVs—also a *Star Trek* technology. The artificial intelligence of voice-responsive computers (think Siri and Alexa) was once a pipe dream technology that now manifests itself, as well as voice recognition and translation.

Circling back in time to Boeing in the late 1970s, our manufacturing technology group would be occasionally tapped to create odd interconnection structures the purpose of which was both unknown and unknowable at the time, though we (or at least I) did have some fun speculating. It was an exhilarating time when we, too, were inventing processes on the fly.

In summary, we owe a debt of gratitude to all the dreamers of new possibilities past, present, and future. Science fiction writers such as those who wrote for *Star Trek,* but also their predecessors such as Jules Verne, Isaac Asimov, Arthur C. Clark, and many others may not have had the technical skills to realize their visions, but they have inspired generations to pursue those visions. Nineteenth century English poet Robert Browning wrote, "Ah, but a man's reach should exceed his grasp, Or what's a heaven for?"

Keep reaching! **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

Cutting the 'Key' to an Unhackable 5G Network

Scientists from Heriot-Watt University have secured six-figure funding from Innovate-UK on a project led by BT to develop practical quantum key distribution (QKD) transmitter and receiver modules for short range terrestrial applications.

QKD is an un-hackable, cutting edge technique for sharing encryption 'keys' between locations using a stream of encoded single photons (quantum bits). The project, called AIRQKD, combines BT's globally leading expertise in building quantum-secure networks using QKD with new techniques for applying quantum security to mobile devices.

The Heriot-Watt team brings essential expertise of practical QKD by leading the design, testing, and construction of the QKD transmitter and receiver prototypes. The team will also support other project partners developing novel single-photon source and detector technologies for the commercial products.

Dr. Ross Donaldson from Heriot-Watt University explains, "Our focus is on how to create a core to this system that will still operate in very tough conditions. Up to now, most quantum communication research has concentrated on the integrity of long-range signals, but this is about delivering a constant service at short distances through the broad range of weather conditions which can cause connection issues.

Prof. Andrew Lord, BT's head of optical network research, said, "We are thrilled to have brought together leading UK partners from industry and academia in the AIRQKD project. This will provide the essential security needed for future 5G applications such as autonomous vehicles."

Other applications for the research will include connected cars, mass manufacturing and Internet of Things devices.

(Source: Heriot-Watt University)

Flex007 Highlights

Sheldahl to Present 'HMI's Evolution to Revolution' at TechBlick 2021 ▶

Human Machine Interface is changing the world and the way that we interact with it. At this year's virtual event, Sheldahl will present HMI's Evolution to Revolution. Expert John Voultos will discuss HMI's beginning, progression, and its revolution in our lives in the future, as well as how flexible circuits and printed electronics will play a part in enabling the technology moving forward.

Researchers Develop New Graphene-based Sensor Technology for Wearable Medical Devices ▶

Researchers at AMBER, the SFI Centre for Advanced Materials and BioEngineering Research, and from Trinity's School of Physics, have developed next-generation, graphene-based sensing technology using their innovative G-Putty material.

Lear Leads Latest Investment Round in Flexible Circuit Maker CelLink ▶

Lear Corporation, a global automotive technology leader in Seating and E-Systems, announced that it is the lead investor for the Series C round of financing in CelLink Corporation, a San Carlos, Calif.-based manufacturer of a new class of flat and flexible circuits that minimize complexity, space and weight.

Rice Engineers Set Sights on Implantable 'Living Pharmacy' ▶

Five Rice University engineering laboratories are part of a $33 million national effort to develop a wireless, fully implantable device that can control the body's circadian clock, halving the time it takes to recover from jet lag and similar disruptions to the body's sleep/wake cycles.

Soft, Comfortable Sensors First to Comprehensively Monitor Pregnant Women, Their Babies Without Wires ▶

Laboring mothers have been wearing the same cumbersome, polyester fetal-monitoring belt for decades. Not only can these belts slip out of place, requiring constant adjustment, they—along with the array of other wires taped to the mother for monitoring—tether the mother to the bed, limiting her ability to walk around or move freely in ways that are more comfortable.

Flexible Thinking: Process Flow for Occam QFN Test Vehicle ▶

Joe Fjelstad teaches the Occam process through a series of steps and images. These solutions can significantly reduce the number of process steps required to manufacture an electronic module or assembly (perhaps by as much as one-third) and in the process making electronic assemblies more reliable and less costly by fundamentally focusing on the elimination of solder and the soldering process.

Arlon's 85HP Receives Official IPC Validation to IPC-4101E-WAM1/43 ▶

Arlon Electronic Materials is pleased to announce that IPC Validation Services officially recognizes Arlon's 85HP laminate as having passed all tests that meets or exceeds the product performance requirements of IPC-4101E-WAM1/43.

Star Trek's Impact on Innovation

Consider This

Feature Column by John Talbot, TRAMONTO CIRCUITS

Gene Roddenberry and his writers and set designers had an enormous task predicting what the future would be like in 2250. The first *Star Trek* television show, "The Original Series," debuted on September 8, 1966 and aired for three seasons on NBC.

- The super futuristic show used a very large "communicator" with a wire mesh antenna as part of the flip phone case. It provided the ever-important "person locator" for beaming back up, including the immortal phrase, "Two to beam up, Scotty." By 2340, the communicator was a gold metallic emblem that you just touched, with seemingly AI ability to know with whom you wanted to communicate with. Of all the future inventions the writers created, the communicator was probably the only one or two that we have even come close to developing.
- Phaser hand-held weapons? Nope, not even close.
- Warp drive? We are still trying to get above 20,000 miles per hour, a monstrously long way to go to light speed and make the leap to warp speed, seven times the speed of light, if that is even possible.
- The AI computers? We have done not a bad job of getting close to what they used.
- The transporter? Well, I will let someone else test it first, not wanting to get my molecules scattered forever.
- My favorite future invention was the "food creator." I'll take a Pittsburgh steak and single malt drink, please. It's a future invention that we have gleefully imagined, but sadly is improbable.

One area remotely possible is "Raise the shields, Mr. Chekov." Future inventions are possible, given some work on electromagnetic plasma fields. The earth's magnetic shield keeps out a large mass of the sun's radiation and forces, so maybe not too far off if we have another 200 plus years of development to catch up on. Many of the enterprise's futuristic inventions are, sorry to say, impossible, knowing what we do today about the laws of physics; but hey, who is to say a new Albert Einstein, 75 years from now, changes our thinking of the laws of physics in a massive way again? It has happened before.

One area remotely possible is "Raise the shields, Mr. Chekov." Future inventions are possible, given some work on electromagnetic plasma fields.

Looking at the printed circuits used by the first *Star Trek* TV shows are of interest. They were clear, with internal traces and I would venture, had circuits inside. Rather rudimentary and not far off what we were manufacturing in 1967, but of course, they performed many more functions than what we could back in the day. Society was still using tubes in their electronic devices at home, such as radios and televisions.

I would have to believe that flex and embedded circuitry was theoretically used. The daily crew uniforms could measure and send information on body functions, a technology that we are advancing, and I suspect will exceed the show's outstanding imagination well before the star date 2234.

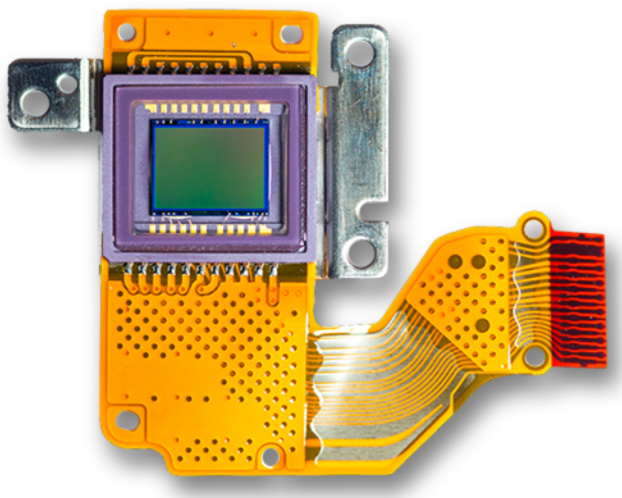
Over the last 60 years, we have seen flex quickly grow with the invention of many new technologies. From its simplistic start as a single-sided print and etch, it has grown to 40 layers of rigid and flexible circuits, proudly going where no circuit has gone before by spreading its arms to interconnect many different individual parts of the overall circuit.

If you ever get the chance to see a camera's flex circuit all folded up with its many spiralia of arms, it is a wonder to behold. Where will flex be in another 220 years? I would guess it will be in much smaller traces, possibly of a superconductor material. The flexible base material may become infused with low cost, man-made diamonds for super high heat conductivity. I can see in my crystal ball, integrated circuits small enough to be embedded right into the base material if Moore's law continues its path to the future.

As flexible circuits are asked to do more, inventors will come to the design table, adding their special niche to the mix. Future electronics is all about smaller, thinner, and more transistors per square nanometer. I know human's desire for creation, and more and more electronics in their lives. Flex circuits will fill the technology gap until flex circuits are truly the invention that the future will need.

Star Trek was important in more ways than just entertainment. It was a first to intentionally feature a multinational cast during the height of a cold war. As well, *Star Trek* featured the first interracial kiss. Having censors on set, trying to hold back a futuristic-thinking Roddenberry would be a tough job. Remember, in 1966 America was struggling with its inability to integrate people of color properly and equally after 300 years of failure. Unfortunately, even today, America is still struggling with its racial past.

The show inspired many future inventors. One huge fan of the first shows was Steve Wozniak who credited watching *Star Trek* and attending *Star Trek* conventions in his youth as a source of inspiration for co-founding Apple



computers, which have probably come as close as anything to the infamous communicator of *Star Trek*. The series drew in inventors—people who think outside the box. Heck, most true inventors with futuristic thinking don't even know there is a design box. One such futuristic past genius, Leonardo DaVinci, comes to mind.

Over the years, one future invention which is close to reality is Scottie's transparent aluminum water tank. Aluminum oxynitride—ALON—is being tested in R&D as it is lighter and stronger than traditional aluminum and it is visibly clear. It was featured in one movie as a container needed to protect the last pregnant whale and save the earth.

The entire body of *Star Trek* television and movie series, with its many, many shows, was always trying to teach us to invent, create, and think of new technologies. However, it also showed humanity was needed and paramount to our future success. Sometimes, I wonder if we could have learned more from the series. FLEX007

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

Printable Circuits Bring Low-cost, High-performance Wearables a Step Closer

Researchers have developed printable inks that enable high-performance inkjet-printed electronic circuits, providing a pathway to wearable devices.

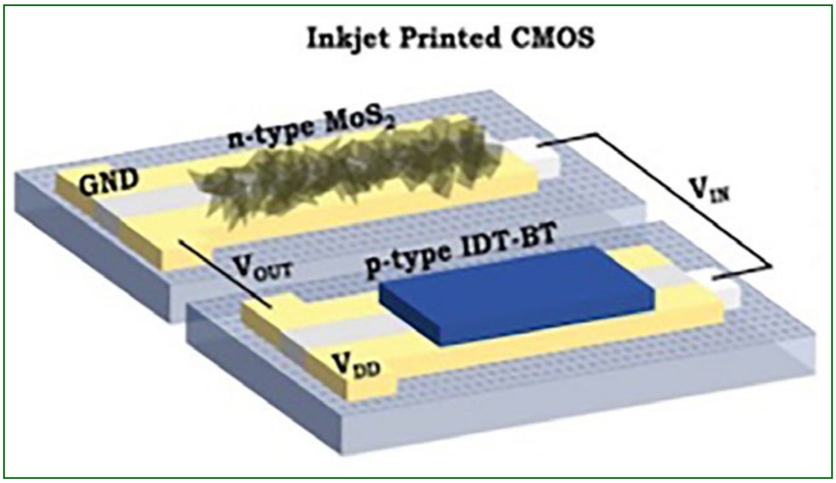
The advantage of producing electronics based on inks is that they are flexible, allowing them to be used in wearable devices like health monitors, body warmers, radio frequency antennas, and electronic textile displays.

The circuits produced by the new electronic inks, which are based on two-dimensional materials, performed as well as commercial organic semiconductors, which are used for applications including next-generation LEDs and solar panels.

Inks that can be printed can also be easily mass-produced, reducing their cost. However, current printable electronics tends to be unstable in air and lack the high performance of organic semiconductors, which could show electrical properties similar to those achieved in standard silicon technologies such as microchips.

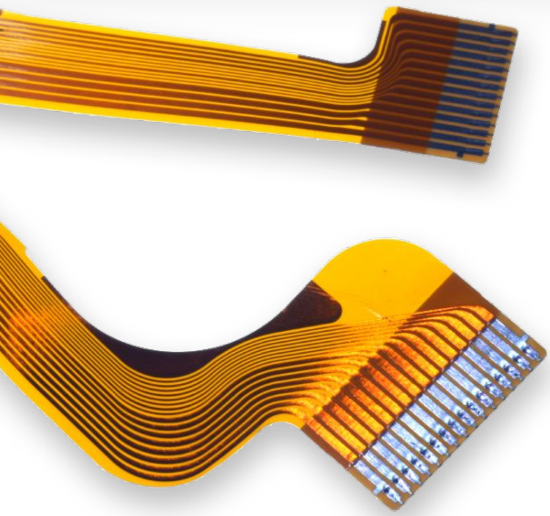
The printable semiconducting inks developed by the team shows superior electrical properties—such as high electron mobility—and air stability, while preserving the versatility of the printing technology. This is significant step toward low-cost high-performance printed and wearable electronics.

The team has so far shown they can print semiconductors—materials that can both conduct and insulate electric charge, depending on the local properties and conditions of the material.



Co-author Professor Roman Sordan, from Politecnico di Milano, said, "Our result represents a first step in the integration of inkjet printed n-type 2D transistors and p-type organic transistors into complementary logic gates which are the backbone of modern digital electronics. We hope this brings us closer to cheap and widely available wearable devices."

(Source: Imperial College London)



1 DFM 101: PCB Materials


Anaya Vardya

One of the biggest challenges facing PCB designers is understanding the cost drivers in the PCB manufacturing process. This article is the first in a series that will discuss these cost drivers (from the PCB manufacturer's perspective) and the design decisions that will impact product reliability.

2 All Systems Go! EM Analysis for Today's System-Level Designs


Brad Griffin

There are two main reasons to do EM analysis: to see if the signals in the design will meet your performance specifications, and to see whether the design has unintended EM interactions in the circuit or system. Since domain-level requirements vary, not all EM solvers are the same.

3 Connect the Dots: A Closer Look at Surface Finish


Matt Stevenson

The final surface finish of a PCB is an important consideration. This coating between your components and the bare board is applied to ensure solderability and protect any exposed copper circuitry. Selecting the right type of surface finish can be daunting, and for good reasons.

4 Standard of Excellence: Dare to Share

We often talk about the value of working closely with your vendors to the point of making them partners. This strategy makes sense. The closer you are to your vendors, the more you help them, the better vendors they will be, and most importantly the better partners they will be. Now let's take that idea to the next level, all the way to the point of a true partnership.

5 Medical, Defense Face Shortage of Multilayer Ceramic Capacitors ▶


Stephen Armstrong

Industrial, medical, and military demand for high-quality, high-voltage multilayer ceramic capacitors (MLCCs) has been hit hard by a shift in production by the world's largest MLCC manufacturers who are focusing on a seemingly insatiable demand for smaller, lower voltage—and in some way—lower-performance MLCCs.

6 Medical, Defense Face Shortage of Multilayer Ceramic Capacitors ▶


Imran Valiani

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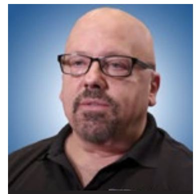
7 Hate PCB Respins? Five Ways to Reduce or Eliminate Respins ▶


Patrick McGoff

Redesigning a printed circuit board is a chore that no one likes. Respins of printed circuit boards cost money, delay the schedule, and just aren't enjoyable for anyone. Yet, many companies are not taking advantage of available tools that can reduce—and in many cases eliminate—PCB respins.

8 Why We Simulate ▶


Bill Hargin

When Bill Hargin was cutting his teeth in high-speed PCB design some 25 years ago, speeds were slow, layer counts were low, dielectric constants and loss tangents were high, design margins were wide, copper roughness didn't matter, and glass-weave styles didn't matter. Dielectrics were called "FR-4" and their properties didn't matter much. A fast PCI bus operated at just 66 MHz. Times have certainly changed.

9 PCB Design Challenges: Designing With DDR ▶

Longtime signal integrity experts Rick Hartley and Barry Olney join the I-Connect007 editorial team for a discussion around DDR and the complications board designers inevitably face when they design for DDR. If the DDR design process is not that much more complicated than that of a typical high-speed board, why does DDR cause design engineers so much grief?

10 EMA Design Automation Expands Operations in the United Kingdom ▶


Dana Korf

EMA Design Automation, a full-service provider and innovator of Electronic Design Automation (EDA) systems solutions, announced it is expanding its operations in the United Kingdom with the addition of Parallel Systems to its sales channel.

Career Opportunities

Career Opportunities

Career Opportunities

Sheldahl

A Flex Company

Sheldahl, a leading provider of flexible interconnect products and electronic materials, is seeking candidates to join their diverse and skilled team.

We are looking for people who demonstrate:

- Intense collaboration
- Passionate customer focus
- Thoughtful, fast, disciplined execution
- Tenacious commitment to continuous improvement
- Relentless drive to win

Positions in America include:

Project Manager – Northfield, MN
Candidate will provide timely cost estimation and project budget definition, be responsible for maintaining customer relations, participate in meetings, etc.

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Program Manager – Specialty Films
Candidate will work with our Specialty Films in the Aerospace, Medical, and Commercial Aviation markets providing timely cost estimation and project budget definition, maintaining customer relations, participate in meetings, etc.

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Business Development Manager – North America
Candidate will provide leadership in the planning, design and implementation of customers' specific business plans and will provide vision, penetration strategies and tactics to executive managers in order to develop and drive external and internal senior-level relationships.

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Sheldahl, a leading provider of flexible interconnect products and electronic materials, is seeking candidates to join their diverse and skilled team.

We are looking for people who demonstrate:

- Intense collaboration
- Passionate customer focus
- Thoughtful, fast, disciplined execution
- Tenacious commitment to continuous improvement
- Relentless drive to win

Positions in Europe include:

Business Development Manager — France
Seeking out-of-the-box thinkers to help us take the ordinary to the extraordinary by cultivating current customer relationships and developing new business opportunities with our European team, based in France.

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Business Development Manager — Germany
Seeking out-of-the-box thinkers to help us take the ordinary to the extraordinary by cultivating current customer relationships and developing new business opportunities with our European team, based in Germany.

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Career Opportunities

INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

View our opportunities at
Insulectro Careers (jobvite.com)

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INDIUM CORPORATION®

Packaging Engineer

Job description: The Packaging Engineer designs and deploys product packaging to ensure product integrity under varying shipping conditions. This individual is responsible for testing, analyzing, and selecting materials for packaging based on durability, function, ease of use and cost effectiveness. The Packaging Engineer helps ensure that packaging complies with all regulatory requirements.

Requirements: Bachelor's degree in engineering, packaging science and at least one year of related work experience. An equivalent combination of education and related work experience may be considered. Demonstrable skills with computer-aided design (CAD) software and other relevant programs.

Indium Corporation is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, the company has global technical support and factories located in China, India, Malaysia, Singapore, South Korea, the United Kingdom, and the USA. Indium Corporation is an Equal Opportunity/Affirmative Action and Minority/Female/Disability/Protected Veteran Employer. We provide a drug-free work environment and a full benefits package.

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Career Opportunities

SIEMENS

Siemens EDA
Sr. Applications Engineer

Support consultative sales efforts at world's leading semiconductor and electronic equipment manufacturers. You will be responsible for securing EM Analysis & Simulation technical wins with the industry-leading HyperLynx Analysis product family as part of the Xpedition Enterprise design flow.

Will deliver technical presentations, conduct product demonstrations and benchmarks, and participate in the development of account sales strategies leading to market share gains.

- PCB design competency required
- BEE, MSEE preferred
- Prior experience with Signal Integrity, Power Integrity, EM & SPICE circuit analysis tools
- Experience with HyperLynx, Ansys, Keysight and/or Sigrity
- A minimum of 5 years' hands-on experience with EM Analysis & Simulation, printed circuit board design, engineering technology or similar field
- Moderate domestic travel required
- Possess passion to learn and perform at the cutting edge of technology
- Desire to broaden exposure to the business aspects of the technical design world
- Possess a demonstrated ability to build strong rapport and credibility with customer organizations while maintaining an internal network of contacts
- Enjoy contributing to the success of a phenomenal team

***Qualified applicants will not require employer-sponsored work authorization now or in the future for employment in the United States. Qualified Applicants must be legally authorized for employment in the United States.*

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U.S. CIRCUIT

Plating Supervisor

Escondido, Calif.-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package. Pay will be commensurate with experience.

Mail to:
mfariba@uscircuit.com

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Career Opportunities

Indium Corporation: Field Sales Representative

Field Sales Representative serves as lead sales contact and customer advocate to maintain existing sales and to drive new qualifications and sales of products and services through effective account management and coordination of efforts throughout Indium Corporation's Metals, Compounds, Solar and Reclaim (MCSR) organization. This position is ideal for a sales- and customer-focused individual with an engineering degree.

- Develop, cultivate, and follow-up with prospective and existing customers to generate orders
- Develop an in-depth expertise of product offerings
- Work to gain insight into customer activities for future R&D developments
- Respond to customer requests for product data, specifications, and service information
- Identify customer requirements, priorities, and opportunities
- Build strong, trusting relationships with key decision-makers and influencers at target accounts
- Gather competitive insight, including pricing, delivery, and performance information
- Visit customer facilities to observe manufacturing processes and exchange information
- Promote industry recognition of Indium Corporation, its products, and its services
- Be a key member of overall team, including worldwide sales organization, product management, operations, engineering, R&D, etc.
- Submit required paperwork in timely manner
- Work within established budget, while increasing market share
- Perform other duties and projects as assigned

Click below for more details on job responsibilities and requirements.

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Our Summit Anaheim, CA, division currently has multiple open positions for planning engineers.

The planner is responsible for creating and verifying manufacturing documentation, including work instructions and shop floor travelers. Review lay-ups, details, and designs according to engineering and customer specifications through the use of computer and applications software. May specify required manufacturing machinery and test equipment based on manufacturing and/or customer requirements. Guides manufacturing process development for all products.

Responsibilities:

1. Accurately plan jobs and create shop floor travelers.
2. Create documentation packages.
3. Use company software for planning and issuing jobs.
4. Contact customers to resolve open issues.
5. Create TDR calculations.
6. Assist in the training of new planning engineers.
7. Review prints and purchase orders.
8. Create stackups and order materials per print/spec.
9. Plan jobs manufacturing process.
10. Institute new manufacturing processes and or changes.

Education/Experience:

1. High school diploma or equivalent
2. Minimum five (5) years' experience in the printed circuit board industry with three (3) years as a planning engineer.
3. Must be able to cooperate and communicate effectively with customers, management, and supervisory staff.
4. Must be proficient in rigid, flex, rigid/flex, and sequential lam designs.

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Career Opportunities

Career Opportunities

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:
- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:
- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:
- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:
- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:
- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Career Opportunities

Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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IPC Instructor

Longmont, CO; Phoenix, AZ; U.S.-based remote

Independent contractor, possible full-time employment

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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Career Opportunities

Career Opportunities

APCT
Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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